Reducing Common-Mode Noise in Two-Switch Forward Converter

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Abstract—This paper addresses the common-mode (CM) electromagnetic interference noise issues in the two-switch forward converter. The two-switch forward converter has low CM noise compared to other topologies because its symmetric primary-side circuit has two out-of-phase $dv/dts$ that cancel each other. However, parasitic capacitances of the circuit significantly affect the symmetry and degrade the noise reduction. Moreover, the secondary-side circuit of the converter is not symmetric and still contributes to the CM noise. In this paper, the parasitic capacitances of the converter are first modeled. Different transformer structures and their parasitic capacitances are characterized. A general balance technique is introduced to further reduce the CM noise of the converter. For each transformer structure, balance can be achieved with proper connection of the windings terminals and control of the parasitic capacitances to minimize the CM noise of the converter. Experimental results validated the proposed techniques.

Index Terms—Common-mode (CM) noise, transformer structure, two-switch forward.

I. INTRODUCTION

TWO-SWITCH forward topology is a competitive candidate in telecom and server applications because of its control simplicity, compact transformer structure, high efficiency, and low common-mode (CM) electromagnetic interference (EMI) noise [1], [2]. In order to achieve higher efficiency and power density, the power transformer of the converter should have compact and fully interleaved winding structure [3], [4]. However, such a compact and interleaved winding structure increases the interwinding capacitance, and thus, has adverse effect on the CM noise emission of the converter. Although a lot of study on CM noise of power converter systems has been studied, most of the discussion focuses on the nonisolated converters [5]–[17]. There is a need to analyze the CM noise propagation in two-switch forward converter and to reduce its CM noise emission.

In a two-switch forward converter, there are two out-of-phase $dv/dts$ with the same magnitude on the primary-side circuit. If their associated parasitic capacitances to ground are same, these two $dv/dts$ will generate out-of-phase CM noise currents that cancel each other completely. However, there are two aspects that are detrimental to the CM noise cancellation in the two-switch forward converter. On one hand, the associated parasitic capacitances may not be the same due to the asymmetric transformer structure and circuit parasitics. On the other hand, from the noise source perspective, the $dv/dt$ on the secondary side still causes CM noise. For a two-switch forward converter with traditional transformer structures, CM noise caused by these two aspects are relatively low compared to other topologies such as phase-shift full bridge. However, with the novel compact and fully interleaved winding structure, the enlarged interwinding capacitance significantly raises the CM noise level so that the benefit of low CM noise is compromised.

This paper focuses on the CM noise modeling and reduction techniques of the two-switch forward converter. CM noise sources of the converter are first identified. Two transformer structures with interleaved windings and their parasitic capacitances are then studied. The distributed parasitic capacitances are modeled as lumped capacitors from the CM noise perspective. The balance technique [5], [6] is then introduced to minimize the CM noise of the converter by achieving the balance conditions, which specify the ratio of noise sources and lumped equivalent CM capacitors. Control of the lumped equivalent CM capacitors is achieved via proper arrangement of the transformer winding structure and by choosing the proper connection between the winding layer terminals and the circuit nodes. Experimental results show that a significant CM noise reduction can be achieved.

II. CM NOISE MODEL OF THE CONVERTER

The topology of two-switch forward converter is shown in Fig. 1. The secondary side of the converter is identical to the forward converter, while on the primary side, two switches are used compared to the single-switch forward converter. In this
two-switch version of forward converter, the two MOSFETs share the same gate drive signal. Fig. 2 shows the voltage waveforms of the converter. $v_g$ is the gate signal of both $S_1$ and $S_2$. Diode $D_3$ conducts when $S_1$ and $S_2$ conduct. When $S_1$ and $S_2$ turn off, $D_3$ stops conducting and $D_4$ commutes the inductor current. On the primary side, the magnetizing current of the transformer forward biases diodes $D_1$ and $D_2$. The transformer primary winding is connected to the input source with opposite polarity. This helps to reset the transformer. After the transformer is fully reset, $D_1$ and $D_2$ become reverse biased. Voltage on the primary winding of transformer is approximately zero. $S_1$ and $S_2$ share the input voltage until they start to conduct in the next switching period.

A. Modeling the CM Noise Sources

$dv/dt$ of the converter is a major cause of CM noise in power supplies. Fig. 3 identifies the major $dv/dt$ of the two-switch forward converter and models them as voltage sources. On the primary side, $S_1$ and $S_2$ are substituted by voltage sources $v_1$ and $v_2$ having the same voltage waveforms. On the secondary side, $D_3$ and $D_4$ are substituted by voltage sources $v_{D3}$ and $v_{D4}$.

These noise sources generate CM noise currents through critical parasitic capacitances to the ground. The CM noise current paths of the converter are indicated in Fig. 3 with dashed lines. All CM noise current loops contain at least one parasitic capacitance from the $dv/dt$ node of the circuit to ground, and such capacitance determines the impedance of the loop at low frequencies.

Some of the CM noise currents propagate from primary-side circuit through primary-side nodes to ground capacitances ($C_1$ and $C_2$ in Fig. 3). They propagate between primary side of the converter and line impedance stabilization network (LISN). The other CM noise current propagates between primary side and the secondary side of the converter through the interwinding capacitances of the transformer. It goes into the ground through the grounding point of the output of the converter and back into LISN on the primary side.

CM noise model of the converter can be derived by simplifying the circuit in Fig. 3. First, LISN can be modeled as two 50-Ω resistors in parallel. Second, the impedance of the input capacitor in the conducted EMI frequency range (150 kHz–30 MHz) is very small even when its equivalent series inductance is taken into account, so that its voltage ripple is very small compared to the $dv/dt$ on the switches. Such a small ripple does not affect the overall CM noise level of the converter and can be ignored in the CM noise modeling process. The input capacitor is treated as a short circuit in the CM noise model. This will result in a fact that $D_1$ is equivalently in parallel with voltage source $v_1$ and can be removed in the model circuit. $D_2$ can be removed for the same reason. On the secondary side, the output LC filter and the parasitic capacitance $C_4$ are both in parallel with voltage source $v_{D4}$ so that they can be removed. After these steps, only $v_{D3}$ and $v_{D4}$ remain on the secondary side, and they can be combined as one noise source $v_3$. The final circuit is shown in Fig. 4. It is the simplified CM noise circuit of the two-switch forward converter without the modeling of the power transformer. It should be noted that although displacement current is introduced on the primary side, it does not contribute to the CM noise emission since it does not go into the LISN. Therefore, the effect of $C_4$ can be ignored.

As shown in Fig. 2, $v_1$ and $v_2$ have identical voltage waveforms when ideal symmetrical structure of the primary-side circuit is assumed. If the transformer windings have perfect coupling (no leakage inductance), the voltage ratio between the primary and secondary windings is approximately the turns ratio $N$. According the Fig. 4, the relation of the three noise sources under these two assumptions is

$$v_1 = v_2 = - \frac{N v_3}{2}. \quad (1)$$
B. Modeling the Interwinding Capacitances of the Transformer

The final and most important step of modeling the CM noise of the converter is to identify and quantify the parasitic capacitances between the power converter and ground. They play an important role in the propagation of CM noise currents. \( C_1 \) and \( C_2 \) in Fig. 3 consist of trace-to-ground and heatsink-to-ground capacitances. They can be identified via measurement or calculation. Interwinding capacitance of the transformer, on the other hand, is distributed in nature, and hence difficult to be identified in terms of its effect on CM noise propagation.

The values and characteristics of interwinding capacitances vary with the transformer winding structures. Fig. 5 shows two typical winding structures in switch-mode power supplies. Both structures have interleaved primary- and secondary-winding layers in order to minimize the winding loss. In this section, transformer structure I is taken as an example to demonstrate the method of modeling the interwinding capacitance of transformer from the CM noise perspective.

In Fig. 5(a), the turns of windings are represented by circles. And the winding direction is denoted with lines. Both primary and secondary windings can be implemented with wires. There are distributed parasitic capacitances between every two adjacent layers, as shown in Fig. 6. In this paper, the parasitic capacitances between windings and core are ignored since it is small compared to winding-to-winding capacitances.

Among the distributed parasitic capacitances between winding layers, those between primary- and secondary-winding layers contribute to CM noise since they provide a CM noise propagation path between the primary and secondary sides. In transformer structure I shown in Fig. 5, there are CM noise currents between layers \( L_2 \) and \( L_3 \), as well as between layers \( L_4 \) and \( L_3 \).

The displacement current between winding layers can be calculated following the same method used in [6]. In order to quantify the total CM noise current going through the parasitic capacitances, the voltage potential distribution along layers is derived based on the assumption that the voltage potential is evenly distributed along the turns of a winding. It is also assumed that the parasitic capacitance is evenly distributed between two layers. When the transformer winding terminals are connected to the circuit in the way shown in Fig. 7, the voltage potentials along layers \( L_2 \), \( L_3 \), and \( L_4 \) can be plotted in Fig. 8.

The difference of \( dv/dt \) between layers causes displacement current on the parasitic capacitances. The total displacement current between layers can be calculated as follows:

\[
i_{BC} = i_{23} = \frac{C_{23}}{2} \left( \frac{dv_2}{dt} - \frac{dv_3}{dt} \right)
\]

\[
i_{AC} = i_{34} = \frac{C_{34}}{2} \left( \frac{dv_1}{dt} - \frac{dv_3}{dt} \right)
\]

where \( C_{23} \) is total capacitances between layers \( L_2 \) and \( L_3 \). \( C_{34} \) is total capacitances between layers \( L_3 \) and \( L_4 \).

In order to have a general CM noise circuit model that is valid for all transformer winding structures, lumped equivalent capacitors across transformer winding terminals are introduced to represent the effects of the distributed parasitic capacitances between layers on CM noise. For example, the capacitances between layers \( L_2 \) and \( L_3 \) are represented by an equivalent capacitor \( C_{BC} \) across transformer terminal B and C from the CM noise perspective. The reason why terminals B and C are chosen is that the voltage potentials of \( L_2 \) and \( L_3 \) are determined by the voltage on B \( (v_2) \) and C \( (v_3) \).
Fig. 9. CM noise model of two-switch forward converter.

The value of the equivalent capacitor is chosen in a way that it causes the same amount of total displacement current as the distributed capacitances do. Since the voltage on B and C are \( v_2 \) and \( v_3 \), the displacement current caused by \( C_{BC} \) can be calculated as follows:

\[
i_{BC} = C_{BC} \left( \frac{dv_2}{dt} - \frac{dv_3}{dt} \right) = \frac{C_{23}}{2} \left( \frac{dv_2/2}{dt} - \frac{dv_3}{dt} \right).
\]

Substitution of (1) into (4) can replace \( v_2 \) with \(-Nv_3/2\). \( C_{BC} \) can be then calculated as follows:

\[
C_{BC} = \frac{N + 4}{2N + 4} \frac{C_{23}}{2}.
\]

Similarly, \( C_{AC} \) is introduced to represent the effect of capacitances between layers \( L_3 \) and \( L_4 \) on CM noise. Displacement current through \( C_{AC} \) is

\[
i_{AC} = C_{AC} \left( \frac{d(-v_1)}{dt} - \frac{dv_3}{dt} \right).
\]

Following the same procedure for calculating \( C_{BC} \), the value of \( C_{AC} \) is

\[
C_{AC} = \frac{N - 4}{2N - 4} \frac{C_{34}}{2}.
\]

With \( C_{AC} \) and \( C_{BC} \) to replace the transformer in Fig. 4, CM noise model of two-switch forward converter is derived, as shown in Fig. 9. The total CM noise can be approximately calculated based on the model and the relation of the voltage sources in (1), assuming that the impedance of the capacitances in the circuit is significantly larger than \( R_{LISN} \)

\[
v_{CM} \approx \frac{R_{LISN}}{2} \left[ \left( C_{AC} + C_{BC} \right) - \frac{N}{2} \left( C_{AC} - C_{BC} + C_1 - C_2 \right) \right] \times \frac{dv_3}{dt}.
\]

III. CM Noise Reduction Via Balance Technique

A. Balance Technique and Balance Conditions

Several noise-reduction techniques have been proposed to reduce the CM noise of the power supplies [5]–[12]. Shielding is a traditional CM noise-reduction method [7]. It can also be combined with other noise-reduction methods to reduce the CM noise [6], [8]. However, shielding layer in the transformer increases the loss and size of the transformer so that it is not preferred for high-efficiency power conversion. Another approach is to achieve symmetry of the CM noise model circuit to create out-of-phase \( dv/dts \) on the same amount of parasitic capacitances [9]–[12]. Achieving symmetry usually requires significant changes on the circuit and increases the complexity and loss. In the two-switch forward converter, the primary side of the converter is symmetric but the secondary side is not. Therefore, additional winding is needed for the secondary side to achieve complete symmetry. The transformer parasitic capacitances need to be controlled to be symmetric too. A more general balance technique reduces the CM noise by controlling the ratio of the \( dv/dts \) and the capacitances to avoid significant changes on the circuit [5], [6]. This technique can be applied to the two-switch forward converter simply via control of the transformer parasitic capacitances.

Fig. 10 shows the equivalent bridge circuit of the CM noise model in Fig. 9. Noise source \( v_3 \) is pushed to the two capacitor branches to form a bridge-type topology. In order to minimize the CM noise voltage on LISN, balance condition specified in (9) should be satisfied so that voltage potentials on the middle points (S, G1, and G2) of all three bridge branches are equal. Consequently, voltage on LISN resistors is zero, which means no CM noise can be measured on LISN. According to (1), the ratio specified in (9) should be equal to 1

\[
\frac{v_{AS}}{v_{SB}} = \frac{v_{AG1}}{v_{BG1}} = \frac{v_{AG2}}{v_{BG2}}.
\]

The grounds G1 and G2 are denoted separately because in practice they are physically separated and connected by wires or chassis of the converter, which introduce parasitic inductances. Such parasitic inductances are not negligible at high frequency so that G1 and G2 do not have the same voltage potential.

If only the CM noise at low frequencies is considered, the two grounds can be treated as one point G. According to the circuit in Fig. 10, balance condition specified in (9) can be achieved by satisfying (10) and (11)

\[
v_1 = v_2 \quad (10)
\]

\[
C_1 - C_2 = \frac{(N + 2)C_{BC} - (N - 2)C_{AC}}{N}. \quad (11)
\]
Equation (11) is relatively easy to achieve by controlling \( C_1 \) or \( C_2 \). Experimental results show that in this way, the CM noise at low frequency can be reduced. However, noise reduction is not as good as at high frequencies.

In order to improve the high-frequency noise reduction, the two ground points G1 and G2 should be considered separately. Equation (11) then becomes two

\[
C_1 = C_2 \\
\frac{C_{AC}}{C_{BC}} = \frac{N + 2}{N - 2}.
\]

Equations (10), (12), and (13) are the balance conditions for CM noise reduction at both low and high frequencies. It can be observed from both the circuit model and the balance conditions that the two-switch forward converter is symmetry on primary-side circuit from the CM noise perspective. However, the secondary-side noise source \( v_3 \) introduces asymmetry in the circuit so that we need to control the ratio of interwinding capacitances of the transformer to cancel its effect on CM noise.

### B. Achieving Symmetry of Primary-Side Noise Sources

It has been assumed that \( v_1 \) and \( v_2 \) are equal in the previous analysis. However, the measurement shown in Fig. 11 indicates that it may not be true in practice.

The asymmetry of \( v_1 \) and \( v_2 \) is due to the parasitic capacitance introduced by the gate drive transformer. In order to drive \( S_1 \), an isolated gate drive circuit is needed. Usually a gate drive transformer is utilized. It introduces interwinding capacitances into the converter, as shown in Fig. 12. Since the input capacitor \( C_{in} \) is considered as a short circuit in the EMI frequency range, the interwinding capacitance of the gate drive transformer is equivalently in parallel with the \( S_1 \) branch and slows down the transient of \( S_1 \).

A compensation capacitor \( C_{comp} \) of the same value can be added in parallel with \( S_2 \) to achieve the symmetry of \( v_1 \) and \( v_2 \). The resulted \( v_1 \) and \( v_2 \) are shown in Fig. 13. The two voltages become identical.

### C. Achieving Balance of Parasitic Capacitances

Balance condition specified in (12) can be achieved by simply adding an external capacitor in parallel with \( C_1 \) or \( C_2 \), whichever is smaller. Balance condition specified in (13) requires a specific ratio of the lumped equivalent interwinding capacitors of the transformer. Although it is possible to add external capacitor in the circuit to change the value of \( C_{AC} \) or \( C_{BC} \), it is not preferred since this method needs additional component. And this capacitor has to be complied with the safety standards so that it is more expensive than a normal one. The leakage inductance of transformer also significantly degrades the effect of cancellation at high frequency [6].

In order to achieve the balance condition specified in (13), the interwinding capacitances can be controlled via the selection of proper winding structure and connection of the winding terminals. In this section, transformer structure I is discussed. Transformer structure II is more complicated and is covered in the next section.

Substitution of (5) and (7) into (13) reveals the required ratio of parasitic capacitances as follows:

\[
\frac{C_{34}}{C_{23}} = \frac{N + 4}{N - 4}
\]
where $C_{L4}$ and $C_{23}$ are capacitances between transformer layers $L_2$, $L_3$, and $L_4$, $L_3$, $L_4$.

The two adjacent winding layers can be modeled as two conductors of the shape of a hollow cylinder, which share the same center, as shown in Fig. 14. The space between them is filled with insulation material. Parasitic capacitance $C_{L,J}$ between them can be calculated as follows:

$$C_{L,J} = \varepsilon_r \frac{2\pi rl}{d} (15)$$

where $\varepsilon_r$ is the permittivity of the insulation material between layers, $l$ is the height of the winding layer, and $d$ is the distance between two winding layers.

According to (15), $C_{23}$ is normally larger than $C_{34}$ due to its larger radius. The balance condition specified in (13) is not met.

In practice, the difference of $C_{23}$ and $C_{34}$ could be more dramatic. The windings are wound from inside-out in manufacturing. Assuming that the same force is applied to wind the wires, the thinner wires will be wound tighter and closer to the adjacent inner winding layer. In transformer structure I, layer $L_3$ has thicker wires than $L_2$ and $L_4$, since it is the secondary winding carrying higher current. Therefore, $L_3$ is wound less tightly to $L_4$, resulting in a larger distance between $L_3$ and $L_4$ than between $L_2$ and $L_3$. According to (15), the parasitic capacitance between layers is inversely proportional to distance. Consequently, $C_{23}$ is much larger than $C_{34}$.

This contradiction can be solved by changing the connection of the transformer winding terminals to the circuit. Previously, winding terminal $P_1$ is connected to node $A$ of the circuit; and $P_2$ is connected to $B$ [see Figs. 4 and 5(a)]. In order to satisfy the balance condition, $P_1$ is connected to $B$; and $P_2$ is connected to $A$. This modification changes the correspondences between the physical parasitic capacitances and the circuit nodes. In the new terminal connection, $C_{23}$ is related to node $B$; and $C_{34}$ is related to node $A$. Consequently, $C_{23}$ and $C_{34}$ exchange their positions in (5), (7), and (14). The capacitance ratio is closer to the ratio specified in (14) compared to the original terminal-connection method.

The merit of choosing proper connection of winding terminals is that the asymmetry of the interwinding capacitances of transformer structure I is utilized to counteract the asymmetry introduced by the secondary-side noise source $v_3$.

After choosing the correct terminal connection, the second step would be to further control the value of $C_{23}$ or $C_{34}$ in order to fully meet the balance condition, if it is necessary. It can be achieved by fine tuning the insulation thickness or choosing proper insulation material with proper permeability too.

IV. MODELING AND REDUCING THE CM NOISE WITH TRANSFORMER STRUCTURE II

A. Equivalent Lumped Capacitances

Fully interleaved transformer structures with spiral windings in order to reduce power losses and volume were proposed in [3] and [4]. In this kind of structures, winding layers are implemented with spiral wires, Printed circuit boards (PCBs), or copper foils. In the structure shown in Fig. 5(b), the primary winding consists of two spiral windings in series, which are implemented with wires. The secondary winding consists of three windings in parallel, which are implemented with PCBs.

Similar to the transformer structure I, CM noise current through structure II can be calculated by integrating the production of distributed voltage and distributed interwinding capacitances. However, parasitic capacitances in this structure are not evenly distributed along the turns of layers. This complicates the calculation process. Fig. 15(b) shows a spiral winding layer. The outer turn in this spiral winding has larger area compared to the inner turns because it has larger diameter. Since the capacitance between two metal sheets is proportional to the area between them, the outer turn has a larger parasitic capacitance.

The superposition theory is introduced to the calculation process. The effect of $dv/dt$ on each layer on CM noise current is separately calculated. When $dv/dt$ on one layer is considered, all the other layers are assumed to have zero voltage potential. A spiral winding layer shown in Fig. 15(b) has $M$ turns with inner radius $r_1$ and outer radius $r_2$. Its voltage potential at the outer terminal is $v_{j1}$ and at inner terminal is $v_{j2}$. The parasitic capacitance per unit area between this layer and the adjacent layers is $\Delta C$. The total capacitance between two layers $C_i = \Delta C (r_i^2 - r_{i-1}^2)$, assuming no space between turns. A displacement current to its adjacent layers caused by the voltage potential change of this layer can be calculated in two steps.
First, displacement current caused by one turn (the mth turn from the inner) of the layer can be calculated as follows:

\[
i_{D,m}(m) = \int_0^{2\pi} \left[ \frac{dv_1}{dt} + \frac{m-1}{M} \left( \frac{dv_1}{dt} - \frac{dv_2}{dt} \right) \right] \, d\theta
\]

\[
+ \frac{\theta}{2\pi M} \left( \frac{dv_1}{dt} - \frac{dv_2}{dt} \right) \times \Delta C \frac{(r_1 + md_w)^2 - (r_1 + (m-1)d_w)^2}{2} \, d\theta
\]

where \( \theta \) is the angle of the circle, \( d_w \) is the width of one turn, and \( d_w = (r_2 - r_1)/M \). The sum of currents of all the turns is the total displacement current caused by the \( dv/dt \) on this layer

\[
i_D = \sum_{i=1}^{M} i_{D,m}(m).
\]

Equations (16) and (17) can be simplified as follows:

\[
i_D = C_1 \left( A_{j1} \frac{dv_1}{dt} + B_{j2} \frac{dv_2}{dt} \right)
\]

where \( C_1 \) is the total parasitic capacitance between this layer and the adjacent layers. \( A_{j1} \) and \( B_{j2} \) are as follows:

\[
A_{j1} = \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/6M^2}{r_2 + r_1}
\]

\[
B_{j2} = \frac{(1/3)r_2 + (2/3)r_1 + (r_2 - r_1)/6M^2}{r_2 + r_1}
\]

Similarly to the transformer structure I, the ways of connecting the transformer layers and connecting winding terminals to nodes of the converter have significant impact on the CM noise level of the converter. One specific terminal connection is chosen to demonstrate how to utilized (18) to calculate the equivalent capacitances \( C_{AC} \) and \( C_{BC} \) in the CM noise model shown in Fig. 9.

In this connection, the inner terminals of \( L_{P1} \) and \( L_{P2} \) are connected together. The terminals \( P1, P2, S1, \) and \( S2 \) of the transformer [see Fig. 5(b)] are connected to the nodes A, B, C, and D of the converter (see Fig. 3).

The terminal voltages of the transformer windings can be derived from the converter circuit. \( P1 = -v1, P2 = v2, S1 = v3, S2 = 0 \). The voltage potential of the inner terminals of \( L_{P1} \) and \( L_{P2} \) is then 0, even when distribution of voltage potential along a winding is assumed. Consequently, voltage potentials of the winding layer terminals are identified and the displacement currents of layers can be calculated with (18).

The total displacement current between layer \( L_{P1} \) and its adjacent layers \( L_{S1} \) and \( L_{S2} \) is the sum of \( i_{D,L_{P1}} \) (caused by the \( dv/dt \) on \( L_{P1} \)), \( i_{D,L_{S1}} \) (caused by the \( dv/dt \) on \( L_{S1} \)), and \( i_{D,L_{S2},L_{P1}} \) (caused by the \( dv/dt \) on \( L_{S2} \) through capacitances between \( L_{S2} \) and \( L_{P1} \))

\[
i_{AC} = i_{D,L_{P1}} + i_{D,L_{S1}} + i_{D,L_{S2},L_{P1}} = (C_{11} + C_{12})
\]

\[
\times \left[ \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/600}{r_2 + r_1} \right] \frac{dt}{dv_1} - \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/24}{r_2 + r_1} \frac{dt}{dv_3} \right].
\]

Similarly, the total current between \( L_{P2} \) and \( L_{S2}, L_{S3} \) is

\[
i_{BC} = (C_{21} + C_{22})
\]

\[
\times \left[ \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/600}{r_2 + r_1} \right] \frac{dt}{dv_2} - \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/24}{r_2 + r_1} \frac{dt}{dv_3} \right].
\]

Equations (21) and (22) can be modified into the form of (4) and (6). Equivalent capacitances \( C_{AC} \) and \( C_{BC} \) for transformer structure II are

\[
C_{AC} = \frac{C_{11} + C_{12}}{r_2 + r_1} \left( \frac{2}{3}r_2 + \frac{1}{3}r_1 - \frac{r_2 - r_1}{6M^2} \right) \frac{N}{N-2}
\]

\[
+ \frac{2}{3}r_2 + \frac{1}{3}r_1 - \frac{r_2 - r_1}{24} \right) \frac{N}{N+2}.
\]

The CM noise model circuit of the converter with the transformer structure II is the same as structure I, but with different equivalent lumped capacitances \( C_{AC} \) and \( C_{BC} \).

B. Controlling the Interwinding Capacitances of Transformer Structure II

Balance method can also be applied to the two-switch forward converter with transformer structure II, and the balance conditions remain the same since the converter has the same CM noise model circuit. The only difference is the equivalent capacitances \( C_{AC} \) and \( C_{BC} \) are changed due to the different transformer structure.

In this structure, \( C_{AC} \) and \( C_{BC} \) are determined by two factors. The first factor is related to the parasitic capacitances between layers. The capacitance between two layers can be calculated as follows:

\[
C_{L,j1} = \frac{\varepsilon}{d} \pi (r_2^2 - r_1^2).
\]

All layers have the same dimension in this structure. Therefore, the only way to change the parasitic capacitance is to change \( d \), the thickness, or the permeability of the insulation material between two layers. In order to achieve the balance condition specified in (13), we can use thinner insulation between layers \( L_{S1}, L_{S2}, \) and \( L_{P1}, \) or thicker insulation between \( L_{S2}, L_{S3}, \) and \( L_{P2} \) to fine tune the parasitic capacitances. However, this requires precise control of the transformer manufacturing to avoid the variation of the parasitic capacitances, which is impractical in production. Consequently, the CM noise reduction is limited.

The secondary factor that determines \( C_{AC} \) and \( C_{BC} \) is related to the dimension and turns of the winding, as well as the terminal voltages. The effect of terminal voltages on equivalent capacitance can be referred to (18). \( A_{j1} \) is always larger than \( B_{j2} \). Its physical meaning is that voltage potential at the outer terminal of the layer has a more significant influence on the total displacement current since the outer turns have larger area.
in dimension. Different terminal connections of the winding layers result in different voltage potentials on layer terminals so that the total displacement current (CM noise current) will change. This change will be reflected in a change of the lumped equivalent capacitance in the CM noise model circuit.

This characteristic provides an opportunity to control $C_{AC}$ and $C_{BC}$ by changing the terminal connections of layers without change of the physical parasitic capacitances. Fig. 16 shows an improved terminal-connection method of the transformer structure. Compared to the previous terminal connection, node B of the converter, which has high $dv/dt$, is connected to the inner terminal on the bottom primary layer. The connections of secondary layer winding terminals are also switched. Consequently, the effects of the $dv/dt$ on CM noises for the corresponding layers are reduced, which results in smaller equivalent capacitances. The values of equivalent capacitances in the CM noise model are changed from (23) and (24) to (26) and (27)

$$C_{AC} = \frac{C_{11} + C_{12}}{r_2 + r_1} \left( \left( \frac{2}{3} r_2 + \frac{1}{3} r_1 - \frac{r_2 - r_1}{600} \right) \right) N$$

$$-2 \left( \frac{1}{3} r_2 + \frac{2}{3} r_1 + \frac{r_2 - r_1}{24} \right) \left( \frac{1}{3} r_2 + \frac{2}{3} r_1 + \frac{r_2 - r_1}{600} \right) N$$

$$C_{BC} = \frac{C_{21} + C_{22}}{r_2 + r_1} \left( \left( \frac{1}{3} r_2 + \frac{2}{3} r_1 + \frac{r_2 - r_1}{600} \right) \right) N$$

$$+2 \left( \frac{1}{3} r_2 + \frac{2}{3} r_1 + \frac{r_2 - r_1}{24} \right) \left( \frac{1}{3} r_2 + \frac{2}{3} r_1 + \frac{r_2 - r_1}{600} \right) N$$

The new terminal connection results in a ratio of $C_{AC}$ and $C_{BC}$ closer to the balance condition specified in (13). Consequently, such a terminal connection reduces the CM noise emission of the converter.

Assuming $C_1 = C_2$. Substitution of (26) and (27) into (8) yields a relation between the ratio of inner, outer radiiuses, and the CM noise magnitude reduction. Fig. 17 shows the CM noise reduction with the improved terminal connection, which varies with the ratio of the inner and outer radiiuses. There is optimal transformer window geometry (ratio of the inner and outer radiiuses) from the CM noise-reduction perspective. However, the geometry of the transformer window is determined from the size and efficiency point of view in practice. With this constraint, the improved terminal connection can only reduce the CM noise by about 8 dB for the specific transformer in our prototype.

Controlling both the parasitic capacitances and terminal connections of the transformer is a better approach to achieve CM noise reduction without the tolerance issue. Asymmetric layer structure is introduced in order to control the parasitic capacitances. According to the balance condition specified in (13), $C_{BC}$ should be smaller than $C_{AC}$. A secondary-side winding layer can be removed to reduce the parasitic capacitance associated with $C_{BC}$, as shown in Fig. 18. The parasitic capacitance associated with $C_{BC}$ is then half of that with $C_{AC}$. Connections of the transformer winding terminals are also changed in order to fine tune $C_{AC}$ and $C_{BC}$. The terminal-connection method in Fig. 18 has been optimized based on a comparison of all possible terminal connections of layers for the specific transformer design used in this paper and the balance condition is achieved.

V. EXPERIMENTAL RESULTS

Two-switch forward prototypes with two transformer structures discussed in this paper were built to verify the proposed CM noise-reduction techniques. Both converters have 400 V input and 12 V output, delivering 200-W output power.

A. Prototype With Transformer Structure I

The prototype for transformer structure I operates at 100 kHz. The core of the transformer is ETD34-N67 from EPCOS. There are 92 turns on the primary and 8 turns on the secondary-side winding. The physical capacitances $C_{23}$ and $C_{34}$ (see Fig. 5) are measured to be 80 and 38 pF, respectively, which verifies the analysis that the outer one is larger than the inner one. $C_2$ is 3 pF and $C_1$ is negligible.

The equivalent capacitances in CM noise model for the original terminal connections can be calculated by (5) and (7). $C_{AC}$ is 23 pF and $C_{BC}$ is 7.5 pF. According to (11), a 24-pF
compensation capacitor can be put in parallel with $C_1$ to achieve low-frequency symmetry. The resulted CM noise is shown in Fig. 19.

To further improve the high-frequency noise reduction, balance conditions specified in (12) and (13) are used instead of (11). A 3-pF capacitor is connected from node B to the ground. The terminal connections of primary windings are switched, as is discussed in Section III-C. The result is shown in Fig. 20. High-frequency CM noise is further reduced. It should be noted that the noise reduction in Fig. 20 is achieved by only switching the terminal connections, without the need of any further adjustment on insulation.

Further CM noise reduction can be achieved by attaining symmetry of primary-side noise sources. The measured interwinding capacitance of the gate drive transformer is 50 pF. With a 50-pF compensation capacitor in parallel with $S_2$, CM noise is further reduced, as shown in Fig. 21.

**B. Prototype With Transformer Structure II**

The prototype for transformer structure II operates at 250 kHz. EQ30–8-N87 from EPCOS is used as the core of this transformer structure. There are 20 turns on the primary and 2 turns on the secondary-side winding. The inner radius is 6.5 mm and outer is 11.5 mm. $C_{11}$, $C_{12}$, $C_{21}$, and $C_{22}$ in Fig. 10 are all 25 pF quantified via measurement. In this prototype, the compensation capacitor has already been put in parallel with $S_2$ to achieve symmetry of the primary-side noise sources.

The effect of improved terminal connection is shown in Fig. 22. Only a 7-dB reduction is achieved at low frequencies. CM noise is further reduced by adjusting the parasitic capacitances with a modification of the insulation thickness. When the sum of $C_{11}$ and $C_{12}$ is adjusted to be 54 pF, and the sum of $C_{21}$ and $C_{22}$ is 45 pF, balance condition is satisfied. The resulted CM noise is shown in Fig. 23.
of insulation. These two methods have similar results in terms of CM noise reduction.

CM noises of the two-switch forward converters are reduced significantly for both transformer structures via the balance technique. However, the high-frequency noise reduction is not as satisfactory as the low frequency. The remaining high-frequency noise peaks are caused by the resonances between the leakage inductance of the transformer and the parasitic capacitances. The leakage inductance was not included in the model used in this paper. A detailed analysis of its effects is covered in [13].

VI. CONCLUSION

In this paper, CM noise modeling and reduction techniques for the two-switch forward converter are discussed. CM noise sources in the converter are first identified. Two typical power transformer structures are studied and their CM noise models are derived. The distributed parasitic capacitances in the transformers are modeled as lumped capacitors for CM noise prediction.

The balance technique is introduced to reduce the CM noise of the converter. Balance conditions for CM noise reduction are derived. On the primary side, the symmetry of a noise source can be achieved by compensating the parasitic capacitance introduced by the gate drive transformer. For the power transformer, it is discovered that both the ways of connecting the transformer winding terminals and the primary parasitic capacitances have significant impacts on the CM noise. Methods of achieving the balance conditions are proposed for both transformer structures to reduce the CM noise. Experimental results show that the CM noise of a two-switch forward converter can be significantly reduced with the proposed methods.

APPENDIX

DERIVATION OF EQUATIONS

Derivation of (18)

The result of the integral in (16) is

\[ i_{Dm}(m) = \pi \left[ \frac{dv_{12}}{dt} + \frac{2m-1}{2M} \left( \frac{dv_{11}}{dt} - \frac{dv_{12}}{dt} \right) \right] \times \Delta C \]

\[ \times \left\{ (r_1 + m d_w)^2 - (r_1 + (m-1) d_w)^2 \right\}. \] (A-1)

Substitution of (A-1) into (17) results in the total displacement current as follows:

\[ i_D = \sum_{1}^{M} i_{Dm}(m) = \Delta C \left( \frac{2}{3} r_2 + \frac{1}{3} r_1 - \frac{r_2 - r_1}{6M^2} \right) \frac{dv_{1}}{dt} + \left( \frac{1}{3} r_2 + \frac{2}{3} r_1 + \frac{r_2 - r_1}{6M^2} \right) \frac{dv_{2}}{dt}. \] (A-2)

Since the total capacitance between two layers \( C_i \) is \( \Delta C \), \( C_i \) can be replace by \( C_i \) so that \( i_D \) becomes

\[ i_D = \sum_{1}^{M} i_{Dm}(m) = C_i \left( \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/6M^2}{r_2 + r_1} \right) \frac{dv_{1}}{dt} + \left( \frac{1/3 r_2 + (2/3) r_1 + (r_2 - r_1)/6M^2}{r_2 + r_1} \right) \frac{dv_{2}}{dt}. \] (A-3)

By defining the coefficients of \( dv_{1}/dt \) and \( dv_{2}/dt \) as \( A_{j1} \) and \( A_{j2} \), (A-3) becomes (18). Equation (18) forms the basis for calculation of displacement currents in a multiple winding layer transformer structure.

Derivation of (21) and (22)

\( i_{DC} \) is the sum of displacement current between \( L_{p1} \) and its adjacent layers \( L_{s1} \) and \( L_{s2} \). It consists of three parts, \( i_{D_{Lp1}}, \)

\[ i_{D_{Ls1}}, \] and \( i_{D_{Ls2}, L_{p1}} \).

\( i_{D_{Lp1}} \) is the displacement current caused by the \( dv/dt \) on \( L_{p1} \). This current can be calculated with (18) when \( v_{j2}, v_{j1}, C_i, \) and \( M \) are given. In the case specified in Section IV-A, \( M \) is 10, \( C_i \) is \( C_{11} + C_{22} \), \( v_{j2} \) and \( v_{j1} \) are outer and inner voltage potentials of layer \( L_{p1} \). They are \(-v_1\) and 0, respectively. Substituting these values into (18) results in

\[ i_{D_{Lp1}} = (C_{11} + C_{22}) \left( \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/600}{r_2 + r_1} \right) \times \frac{d(-v_1)}{dt}. \] (A-4)

\( i_{D_{Ls1}} \) is the displacement current caused by the \( dv/dt \) on \( L_{s1} \). It can be calculated with (18), where \( v_{j2}, v_{j1}, C_i, \) and \( M \) are \( v_3, 0, C_{11}, \) and 2, respectively

\[ i_{D_{Ls1}} = -C_{11} \left( \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/24}{r_2 + r_1} \right) \times \frac{d(-v_3)}{dt}. \] (A-5)

It should be noted that there is a minus sign for the current because it is from secondary side to primary side of the transformer.

\( i_{D_{Ls2}, L_{p1}} \) is the displacement current caused by the \( dv/dt \) on \( L_{s2} \) through capacitances between \( L_{s2} \) and \( L_{p1} \). It can
be calculated with (18), where \( v_{j2}, v_{j1}, C_1, \) and \( M \) are \( v_3, 0, C_{22}, \) and 2, respectively

\[
i_{\text{D_La1}} = -C_{22} \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/24}{r_2 + r_1} \frac{d(-v_3)}{dt} .
\]

The sum of (A-4), (A-5), and (A-6) is (21). Equation (22) is derived in the same way. The only differences between (21) and (22) are that the primary \( dv/dt \) is changed from \(-v_1\) to \( v_2\), and that the total capacitances are changed from \((C_{11} + C_{22})\) to \((C_{21} + C_{22})\).

**Derivation of (23) and (24)**

When a lumped equivalent capacitor is used to model the effect of parasitic capacitances on CM noise, the displacement current through this capacitor is specified in (6). It should be equal to (21)

\[
C_{AC} \left( \frac{d(-v_1)}{dt} - \frac{dv_3}{dt} \right) = (C_{11} + C_{12})
\]

\[
\times \left[ \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/600}{r_2 + r_1} \frac{d(-v_1)}{dt} \right. \\
\left. - \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/24}{r_2 + r_1} \frac{dv_3}{dt} \right].
\]

(A-7)

Substitution of (1) into (A-7) can replace \( v_1 \) with \(-Nv_3/2\)

\[
C_{AC} \left( \frac{d(Nv_3/2)}{dt} - \frac{dv_3}{dt} \right) = (C_{11} + C_{12})
\]

\[
\times \left[ \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/600}{r_2 + r_1} \frac{d(Nv_3/2)}{dt} \right. \\
\left. - \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/24}{r_2 + r_1} \frac{dv_3}{dt} \right].
\]

(A-8)

Further removing \( dv_3/dt \) from (A-8) can have the value of \( C_{BC} \) as in (23). Equation (24) can be derived based on (4) and (22) in the same way.

**Derivation of (26) and (27)**

They can be derived in the same way as (23) and (24). The new displacement current \( i_{AC} \) and \( i_{BC} \) for this improved winding terminal connection (see Fig. 16) are first derived following the same way used to derived (21) and (22)

\[
i_{AC_{\text{new}}} = (C_{11} + C_{12})
\]

\[
\times \left[ \frac{(2/3)r_2 + (1/3)r_1 - (r_2 - r_1)/600}{r_2 + r_1} \frac{d(-v_1)}{dt} \right. \\
\left. - \frac{(1/3)r_2 + (2/3)r_1 + (r_2 - r_1)/24}{r_2 + r_1} \frac{dv_3}{dt} \right].
\]

(A-9)

\[
i_{BC_{\text{new}}} = (C_{11} + C_{12})
\]

\[
\times \left[ \frac{(1/3)r_2 + (2/3)r_1 + (r_2 - r_1)/600}{r_2 + r_1} \frac{dv_2}{dt} \right. \\
\left. - \frac{(1/3)r_2 + (2/3)r_1 + (r_2 - r_1)/24}{r_2 + r_1} \frac{dv_3}{dt} \right].
\]

(A-10)

Following the same way of deriving (23) and (24), by comparing (A-9) with (6), and (A-10) with (4), the lumped equivalent capacitors \( C_{AC} \) and \( C_{BC} \) for this structure can be derived as (26) and (27).

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