Parasitic Inductance Modeling and Reduction for Wire-bonded Half-bridge SiC Multichip Power Modules

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***Abstract*- This paper firstly developed an inductance model that includes the parasitic mutual inductance between parallel current path segments for SiC multichip power modules. Based on the developed model, the SiC multichip module's transient response was analyzed, important parasitic inductances were identified. The layout was improved based on the transient analysis. The improved package layout can reduce the parasitic inductance without increasing the fabrication difficulty. Experiments were conducted to validate the reduction of parasitic inductances. The parasitic ringing and the crosstalk effect were significantly reduced with the proposed technique. The thermal performance was also improved with the proposed layout.**

Keywords—SiC power module, parasitic inductance, mutual inductance, parasitic ringing

I. Introduction

Wide bandgap (WBG) devices can achieve higher efficiency, higher power density, and higher operating temperature [2] than Si devices. Among WBG power devices, SiC MOSFETs have characteristics such as high breakdown voltage, high operating temperature, and low switching power loss, so they are widely used to replace Si IGBTs in high power applications such as electric vehicle and aviation industry. Due to the limited current capability of a single SiC MOSFET chip [3][4], the paralleled multichip structure is typically adopted in SiC MOSFET packages. The wire-bonded direct bond copper (DBC) packing technology is the most popular in multichip power modules. However, the bond wires and 2D layout have large parasitic inductance resulting in severe voltage overshoots and oscillations at high di/dt switching. This leads to high switching power loss, high voltage stress, and electromagnetic interference (EMI) issues [2][28][29].

The parasitic inductance in power modules has been modeled in many papers. In [7], the current commutation loop (CCL) is used to model parasitic inductance, and the switching cell concept is used in the reduction of CCL loop area and the parasitic inductance. The loop inductance model was also used in [9] to develop a multiloop design technique in multilayer PCB prototypes. However, the mutual inductance between paralleled current path segments is not included in the model. The parasitic inductance is extracted via finite element analysis (FEA) software in [10][25] for the simulations of the voltages and currents outside the module. [10] shows that the simulated overshoot is 14% smaller than the measured. A measurement-based parasitic inductance extraction technique is proposed in [26] for multichip power modules. The parasitic inductance of each parallel path segment was measured using an impedance analyzer. However, the mutual inductance between parallel path segments is still not modeled. A detailed parasitic inductance model that includes mutual inductance was developed in [19] for the planar bus bar of an IGBT H bridge. The relationship between current paths and parasitic inductance was firstly illustrated in a bus bar, but the mutual inductance between the parallel current path segments inside multichip power modules has not been thoroughly investigated.

The reduction of parasitic inductance is mostly realized by reducing the CCL area. Some general design guidelines were summarized in [7]. [8] adopted the switching cell concept in [7] to reduce the parasitic inductance. Bond wires and the planar hybrid structure was proposed in [20]. PCB and DBC hybrid structures were proposed in [17] and [21] – [23]. Mutual inductance between the partial inductance of the same power loop is analyzed in [17] and [21] – [23]. A twisted loop structure is designed to reduce loop inductance. However, the mutual inductance between parallel power loops is not considered. The mutual inductance between the driving loop and the power loop is investigated in [17]. It is discovered in [18] that interleaving half-bridge (HB) units can reduce parasitic inductance, but the resulting structure requires complicated bus bar design with DC capacitors on each unit. The mutual inductance between loops was discussed in [9] for multilayer PCB trace loop design but not for 2D power module design. [6] [10] [12] - [16] showed that planar and 3D structures could reduce parasitic inductance by eliminating bond wires, but they significantly increase the fabrication difficulty. The DBC with a wire-bonded structure is still the most economical and suitable package technology for SiC multichip power modules at this time.

Different from the above techniques, the mutual inductance among the parallel current path segments will be investigated in this paper. A parasitic inductance model is developed to predict voltage overshoots and oscillations during switching transients. A wire-bonded package layout is proposed to reduce parasitic inductance based on the developed model.

II. Develop the Parasitic Inductance Model

A. Inductance Model

A commercial HB SiC multichip power module layout is shown in Fig.1 (a). The module has a maximum power rating of 1200 V / 300 A. There are two cells in parallel. In each cell, both top and bottom switches have three parallel SiC MOSFET and three antiparallel SiC Schottky diode chips. There are equivalently six HBs in parallel. The gate drivers are connected to high gates (HG) and high source (HS), and low gates (LG) and low source (LS) pins. The schematic is in Fig.1 (b). In Fig. 1 (a), the output terminal branches are not in CCL, so its parasitic inductance will not be analyzed.

In Fig. 1 (a), each paralleled HB consists of three current path segments labeled with red, black, and green. Fig. 2 shows the side view. For clarity, gate drive loops and gate resistors are

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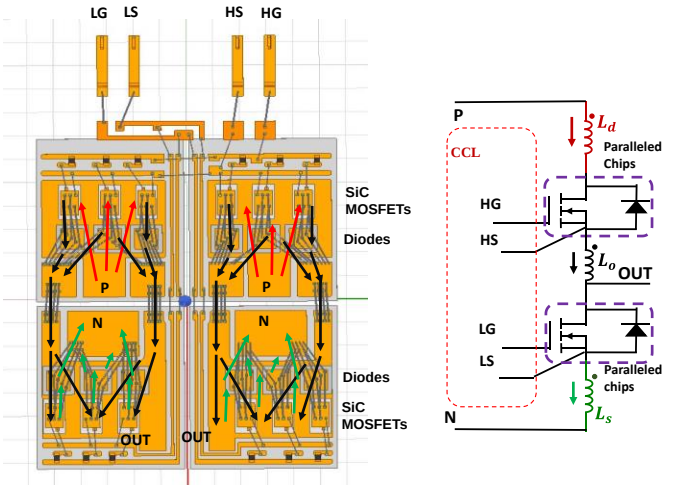
hidden. Different materials are labeled with different colors. Because the copper plane that connects to the negative terminal (N) overlaps the copper plane that connects to the output terminal OUT, a different color (brown) is used for the overlap. As shown in Figs. 1 and 2, the 1st path segment (red arrow) with inductance L_d is from positive terminal (P) to the DBC copper plane, and to the drains of top switches and the cathodes of top diodes. The 2nd path segment (black arrow) with inductance L_O is from the bond wires to the DBC copper plane, to the output terminal OUT, the drains of low switches, and the cathodes of low diodes. Finally, the 3rd path segment (green arrow) with inductance L_S is from the bond wires, to the DBC copper plane and to terminal N. A partial and mutual inductance modeling technique is used to model the total parasitic inductance. The inductance includes the self-inductance of each path segment and the mutual inductance between each pair. The current paths for each paralleled HB are different in Fig. 1 (a).



(a) (b)

Fig.1 Commercial SiC multichip power module layout: (a) top view with the case and terminals hidden, (b) schematic with parasitic inductance.

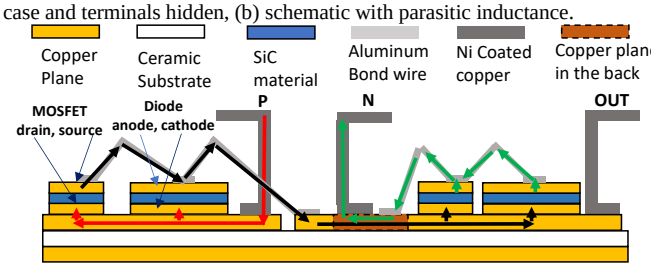


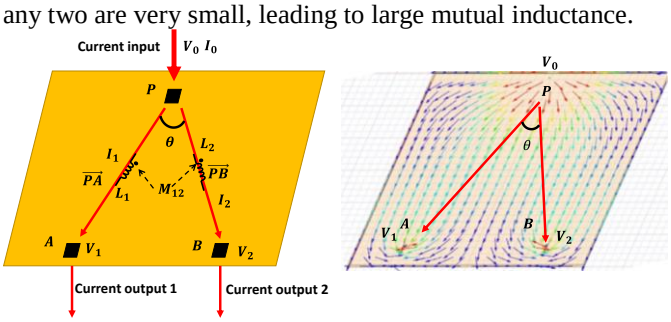
Fig. 2 Illustration of the three conduction path segments of the current commutation loop inside the power module with side view.

To investigate the mutual inductance between paralleled path segments, a model is developed in Fig.3. Points P, A, and B have voltage potentials V_0, V_1 and V_2 on a copper plane. The mutual inductance between current path segments $\overrightarrow{PA}$ and $\overrightarrow{PB}$ can be calculated as:

$$M_{12} = \frac{\iint \mu_0 H_1 H_2 \cos\theta \, dV}{I_1 I_2} \quad (1)$$

where H_1 and H_2 are the magnetic field generated by I_1 and I_2 respectively and the position angle between $\overrightarrow{PA}$ and $\overrightarrow{PB}$ is θ.

In a traditional multichip power module in Fig. 1 (a), the paralleled chips are very close to each other, and the parallel current segments share the same conductors such as copper planes and some bond wires. As a result, the angles between any two are very small, leading to large mutual inductance.



(a) (b)

Fig.3 Current paths on a copper plane with one input and two outputs: (a) current paths, and (b) simulated current vectors.

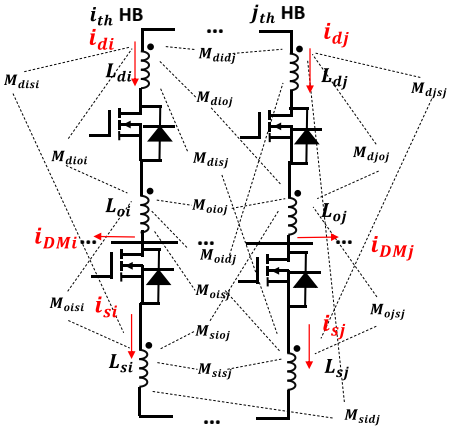


Fig.4 Self and mutual inductance of paralleled HB i and j.

In the inductance model in Fig. 4, L_{di}, L_{oi}, and L_{si} are the self-inductance of the three path segments of the HB i in Fig. 2, respectively. The mutual inductance $M_{(d,o,s)\,i\,(d,o,s)\,j}$ between any two path segments of HB i and j are also shown in Fig.4. Because the drains of switches are bonded on a low impedance DBC copper plane connected to OUT, there is no inductance between the drains. The induced voltages across different inductances during switching transients are different because the parasitic self and mutual inductances of each path segment are different. Each HB includes a top and a bottom branch. The voltage difference between parallel branches leads to inter-branch current in Fig. 4, resulting in an unbalanced dynamic current: if the currents flowing through the top and bottom switches of the i^{th} and j^{th} HBs are represented with i_{di} , i_{si}, and i_{dj} , i_{sj}, because of the inter-branch current, they are not equal. In Fig. 4, the parasitic inductance can be represented with self and mutual inductance matrices $\boldsymbol{L_i}$ and $\boldsymbol{M_{ij}}$:

$$\boldsymbol{L_i} = \begin{bmatrix} L_{di} & M_{dioi} & M_{disi} \\ M_{oidi} & L_{oi} & M_{sioi} \\ M_{sidi} & M_{oisi} & L_{si} \end{bmatrix} \quad (2)$$

$$\boldsymbol{M_{ij}} = \begin{bmatrix} M_{didj} & M_{dioj} & M_{disj} \\ M_{oidj} & M_{oioj} & M_{oisj} \\ M_{sidj} & M_{sioj} & M_{sisj} \end{bmatrix} \quad (3)$$

$\boldsymbol{L_i}$ consists of the self-inductance of each path segment and the mutual inductance between any two path segments within HB i. $\boldsymbol{M_{ij}}$ consists of all the mutual inductance between any two path segments on HB i and HB j. During the transient, the voltage drops on the parasitic inductance of the i^{th} HB is:

$$\begin{bmatrix} V_{di} \\ V_{oi} \\ V_{si} \end{bmatrix} = \boldsymbol{L_i} \cdot d \begin{bmatrix} i_{di} \\ i_{di} \\ i_{si} \end{bmatrix} /dt + \boldsymbol{M_{i1}} \cdot d \begin{bmatrix} i_{d1} \\ i_{d1} \\ i_{s1} \end{bmatrix} /dt + \ldots \boldsymbol{M_{ij}} d \begin{bmatrix} i_{dj} \\ i_{dj} \\ i_{sj} \end{bmatrix} /dt \quad (4)$$

The transient responses of the power module can be discussed based on the inductance model in the analysis below.

B. Turn-off Transient Analysis

The turn-off transient of the top switches is firstly analyzed. Fig. 5 (a) shows the turn-off transient of the i^{th} HB in four stages. L_{wire} is the inductance of the conductors between the DC source and the DC-link capacitors. ESL and ESR are the equivalent series inductance and resistance of the DC capacitors C_{DC}, respectively. L_{lead} is the parasitic inductance of the interconnections such as lead wires, PCB traces and the external bus bar between the DC capacitors and the module terminals. The physical structure which results in L_{lead} is shown later in Fig. 8. The inductive couplings between L_{lead} and the CCL segments inside the module are very small, so they can be ignored. This assumption will be validated in Section II-D.

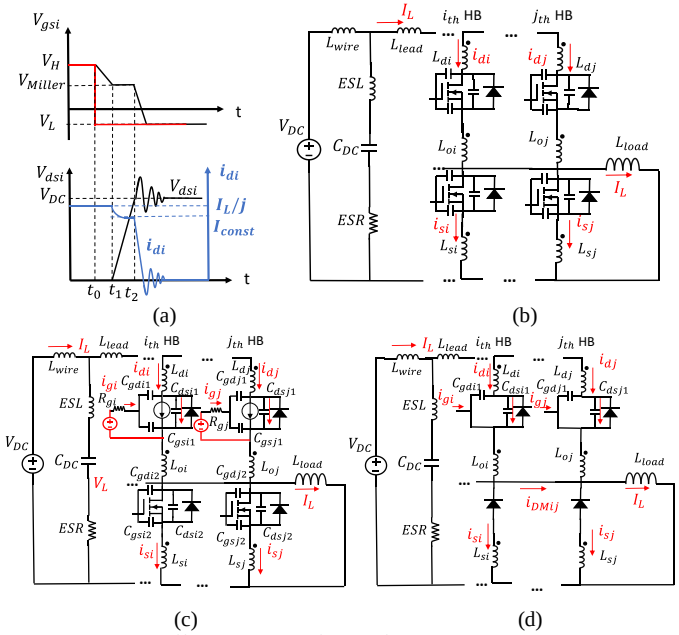


Fig.5 (a) The turn-off transient waveforms of the top switch and the equivalent circuits during: (b) stage 1, (c) stage 2 and 3 (d) stage 4.

Stage 1: before top switches are turned off ($< t_0$).

In Fig. 5 (b), the load current I_L is the sum of the current i_{di} in all branches. The currents are given by:

$$\sum_1^j i_{di} = I_L \quad (5)$$

$$i_{s1} = i_{s2} = \cdots = i_{sj} = 0 \quad (6)$$

In multichip power modules, the current in each branch is nearly equal to I_L/j at the steady-state and I_L is constant due to the large load inductance.

Stage 2: before Miller plateau ($t_0 - t_1$).

The gate voltage V_{gsi} of top switches decreases after the driving signal switches from high V_H to low V_L. The drain to source voltage V_{dsi} of the top switches is still low. The MOSFET operates in the Ohmic region. The drain current is given by:

$$i_{chi} = i_{di} = K_m\left(V_{gsi} - V_{thi}\right)V_{dsi} \quad (7)$$

where i_{chi} and V_{thi} are the channel current and top switch threshold voltage in the i^{th} HB; K_m is transconductance in A/V^2. i_{di} is controlled by V_{gsi}, not affected by the parasitic inductance.

Stage 3: voltage rising stage ($t_1 - t_2$).

At t_1, the drain to source voltage of the top switches rises, and the gate voltage reaches the Miller plateau. The MOSFETs operate in the saturation region. g_m is transconductance in A/V.

$$i_{chi} = g_m\left(V_{gsi} - V_{thi}\right) \quad (8)$$

$$i_{di} = i_{chi} + C_{ossi1}\frac{dV_{dsi}}{dt} \quad (9)$$

$$C_{ossi1} = C_{gdi1} + C_{dsi1} \quad (10)$$

$$i_{gi} = C_{gdi1} \cdot \left(\frac{dV_{gsi}}{dt} - \frac{dV_{dsi}}{dt}\right) + C_{gsi1}\frac{dV_{gsi}}{dt} \quad (11)$$

$$i_{si} = -C_{ossi2}\frac{dV_{dsi}}{dt} \quad (12)$$

$$C_{ossi2} = C_{gdi2} + C_{dsi2} \quad (13)$$

At Miller plateau, $dV_{gsi}/dt \approx 0$, from (11):

$$\frac{dV_{dsi}}{dt} = -\frac{i_{gi}}{C_{gdi}} \quad (14)$$

The gate current i_{gi} and Miller voltage V_{Miller} are given by:

$$i_{gi} = \frac{V_L - V_{gsi}}{R_{gi}} \quad (15)$$

$$V_{Miller} = V_{gsi} = \frac{I_L}{j \cdot g_m} + V_{thi}. \quad (16)$$

where R_{gi} is the gate resistance of the top switch of the i^{th} HB. From (8) (9) (12) (14) and (15), during the Miller plateau period, $\frac{dV_{dsi}}{dt}$, i_{di}, and i_{si} are constant [30]. The drain current of the i^{th} HB is given by:

$$i_{di} = I_{const} = \frac{I_L}{j} + i_{si} \quad (17)$$

where, i_{si} is negative during this stage in (12). Therefore, the drain current is a constant value smaller than $\frac{I_L}{j}$, as shown in Fig. 5 (a). Because the parasitic inductance is much smaller than the load inductor, it has little impact on the device current.

Stage 4: ringing stage ($> t_2$)

In Fig. 5 (d), the ringing stage starts when the bottom diodes start to conduct currents (i_{si}<0). The magnitude of the ringing depends on the initial current in the parasitic inductance and the initial voltage of the output capacitance.

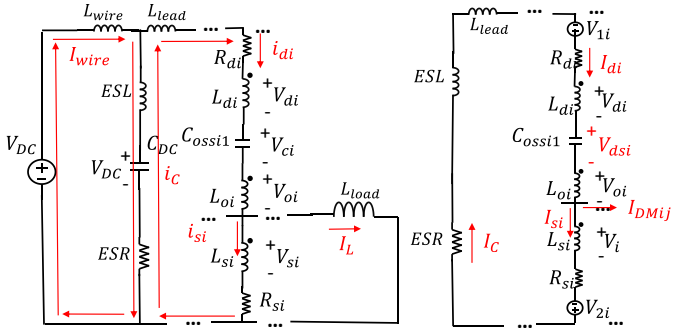


Fig.6 Equivalent circuits during the ringing stage: (a) time domain and (b) frequency domain.

In Fig. 6 (a), R_{di} and R_{si} are the total resistance of the path segments and the diode which i_{di} and i_{si} flowing through. The impedance of the DC link capacitor is in parallel with the power module. The DC link capacitors include high frequency (HF) film and ceramic capacitors with small ESL and ESR. Their small impedance bypass HF currents and decouple the power module from the DC source. As a result, the frequency domain circuit without L_{wire} and V_{DC} in Fig. 6 (b) will be analyzed later.

In Fig. 6 (b), the initial currents in the parasitic inductances and initial voltages on output capacitances are represented with equivalent voltage sources V_{1i} and V_{2i} for top and bottom branches, respectively.

By solving (9), (12), (14), and (17), the initial currents at t_2 in the parasitic inductance are:

$$i_{di}(t_2) = \frac{I_L}{j} + i_{si}(t_2) \tag{18}$$

$$i_{si}(t_2) = C_{ossi2} \cdot \frac{V_L - V_{Miller}}{R_{gi} C_{gdi}} \tag{19}$$

The initial voltages on the output capacitance of the top switch can be calculated from Fig.6 (a) with KVL:

$$V_{ci}(t_2) = V_{DC} - [i_{di}(t_2)R_{di} + i_{si}(t_2)R_{si} + i_C(t_2)ESR + V_{lead}(t_2) + V_{di} + V_{oi} + V_{si}], \tag{20}$$

where,

$$i_C(t_2) = \sum_{i=1}^{j} i_{di}(t_2) \tag{21}$$

$$\begin{bmatrix} V_{di} \\ V_{oi} \\ V_{si} \end{bmatrix}_{t_2} = \boldsymbol{L_i} \cdot d \begin{bmatrix} i_{di}(t_2) \\ i_{di}(t_2) \\ i_{si}(t_2) \end{bmatrix} /dt + \boldsymbol{M_{i1}} \cdot d \begin{bmatrix} i_{d1}(t_2) \\ i_{d1}(t_2) \\ i_{s1}(t_2) \end{bmatrix} /dt + \ldots \boldsymbol{M_{ij}} d \begin{bmatrix} i_{di}(t_2) \\ i_{di}(t_2) \\ i_{si}(t_2) \end{bmatrix} /dt \tag{22}$$

$$V_{lead}(t_2) = (ESL + L_{lead}) \cdot \frac{di_C(t_2)}{dt}, \tag{23}$$

V_{lead} is the total voltage on L_{lead} and the ESL. With the initial conditions, V_{1i} and V_{2i} are calculated from (24) and (25).

$$V_{1i} = \left(\left(\boldsymbol{L_i} \cdot \begin{bmatrix} i_{di}(t_2) \\ i_{di}(t_2) \\ i_{si}(t_2) \end{bmatrix} \right)^T + \left(\boldsymbol{M_{i1}} \cdot \begin{bmatrix} i_{d1}(t_2) \\ i_{d1}(t_2) \\ i_{s1}(t_2) \end{bmatrix} \right)^T + \cdots \left(\boldsymbol{M_{ij}} \cdot \begin{bmatrix} i_{di}(t_2) \\ i_{di}(t_2) \\ i_{si}(t_2) \end{bmatrix} \right)^T \right) \cdot \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} + \frac{V_{ci}(t_2))}{s}, \tag{24}$$

$$V_{2i} = \left(\left(\boldsymbol{L_i} \cdot \begin{bmatrix} i_{di}(t_2) \\ i_{di}(t_2) \\ i_{si}(t_2) \end{bmatrix} \right)^T + \left(\boldsymbol{M_{i1}} \cdot \begin{bmatrix} i_{d1}(t_2) \\ i_{d1}(t_2) \\ i_{s1}(t_2) \end{bmatrix} \right)^T + \cdots \left(\boldsymbol{M_{ij}} \cdot \begin{bmatrix} i_{di}(t_2) \\ i_{di}(t_2) \\ i_{si}(t_2) \end{bmatrix} \right)^T \right) \cdot \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \tag{25}$$

Based on Fig. 6 (b), the drain-to-source voltages of the top switches are given by (26).

$$\begin{bmatrix} V_{ds1}(s) \\ \vdots \\ V_{dsj}(s) \end{bmatrix} = \begin{bmatrix} V_{11} + V_{21} \\ \vdots \\ V_{1j} + V_{2j} \end{bmatrix} - \left(\begin{bmatrix} V_{d1}(s) + V_{o1}(s) + V_{s1}(s) \\ \vdots \\ V_{dj}(s) + V_{oj}(s) + V_{sj}(s) \end{bmatrix} - \begin{bmatrix} I_{d1}(s)R_{d1} \\ \vdots \\ I_{dj}(s)R_{dj} \end{bmatrix} - \begin{bmatrix} I_{s1}(s)R_{s1} \\ \vdots \\ I_{sj}(s)R_{sj} \end{bmatrix} - \begin{bmatrix} I_C(s) \cdot (s \cdot (ESL + L_{lead}) + ESR) \\ \vdots \\ I_C(s) \cdot (s \cdot (ESL + L_{lead}) + ESR) \end{bmatrix} \right) \tag{26}$$

where,

$$\begin{bmatrix} I_{d1}(s) \\ \vdots \\ I_{dj}(s) \end{bmatrix} = s \begin{bmatrix} C_{oss11} \cdot V_{ds1}(s) \\ \vdots \\ C_{ossj1} \cdot V_{dsj}(s) \end{bmatrix} \tag{27}$$

$$\begin{bmatrix} V_{di}(s) \\ V_{oi}(s) \\ V_{si}(s) \end{bmatrix} = \boldsymbol{L_i} \cdot s \begin{bmatrix} I_{di}(s) \\ I_{di}(s) \\ I_{si}(s) \end{bmatrix} + \boldsymbol{M_{i1}} \cdot s \begin{bmatrix} I_{d1}(s) \\ I_{d1}(s) \\ I_{s1}(s) \end{bmatrix} + \ldots \boldsymbol{M_{ij}} \cdot s \begin{bmatrix} I_{dj}(s) \\ I_{dj}(s) \\ I_{sj}(s) \end{bmatrix} \tag{28}$$

Because of the unbalanced inductance in each parallel HBs, the initial conditions of each HBs are different. The DM current I_{DMij} flowing between the i^{th} HB and the j^{th} HB due to different initial voltages can be calculated as:

$$I_{DMij}(s) = \frac{V_{2j} - V_{2i}}{s(L_{si} + L_{sj} - 2M_{sisj}) + R_{si} + R_{sj}} + \frac{V_{1i} - V_{1j}}{sL_{dij} + s \cdot 2(M_{dij}) + \frac{1}{sC_{dij}} + R_{dij}} \tag{29}$$

Where $L_{dij}, M_{dij}, C_{dij}$ and R_{dij} represent the sum of the impedance of the current segments where I_{di} and I_{dj} flow. $L_{dij} = L_{di} + L_{oi} + L_{dj} + L_{oj}$. $M_{dij} = M_{dioi} + M_{djoj} - M_{didj} - M_{dioj} - M_{oidj} - M_{oioj}$. $C_{dij} = \frac{C_{ossi1} C_{ossj1}}{C_{ossi1} + C_{ossj1}}$. $R_{dij} = R_{di} + R_{dj}$.

For the i^{th} HB:

$$I_{si}(s) = I_{di}(s) - I_{DMij}(s) \tag{30}$$

Because there are $3 \times j$ unknown parameters in (26), and $3 \times j$ equations from (26) to (30), the voltage and current of each switch can be solved.

C. Turn-on Transient Analysis

The analysis of turn-on transient is similar to that of the turn-off transient. Fig. 7 (a) shows the turn-on transient of the top switch in the i^{th} HB.

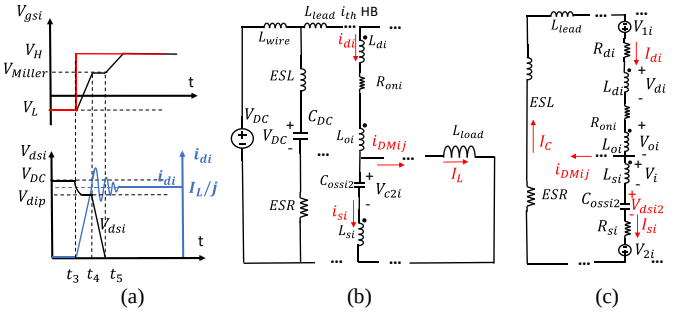


Fig.7 The turn-on transient of the top switch: (a) time-domain waveforms, (b) time-domain equivalent circuit and (c) frequency-domain equivalent circuit

Stage 1: before top switches are turned on ($< t_3$).

The circuit is the same as Fig. 5 (b). The load current flows through the antiparallel diodes of the bottom switches.

$$\sum_1^j i_{si} = -I_L \tag{31}$$

$$i_{d1} = i_{d2} = \cdots = i_{dj} = 0 \tag{32}$$

Stage 2: current rising stage ($t_3 - t_4$).

During the current rising stage, the equivalent circuit is the same as Fig. 5 (c). The MOSFETs are operating in the saturation region. The channel current is governed by (8). The drain to source voltage of the top switches due to the power loop parasitic inductance is,

$$V_{dsi}(t_3) = V_{DC} - [i_{di}(t_3)R_{di} + i_{si}(t_3)R_{si} + i_C(t_3)ESR + V_{lead}(t_3) + V_{di} + V_{oi} + V_{si}] \tag{33}$$

where,

$$V_{lead}(t_3) = (ESL + L_{lead}) \cdot \frac{d(\sum_{i=1}^{j} i_{si}(t_3))}{dt} \tag{34}$$

V_{di}, V_{oi}, V_{si} are governed by (4). The voltage drops caused by the parasitic inductance in this stage have little impact on i_{di}.

Stage 3: voltage decreasing stage ($t_4 - t_5$).

After i_{di} reaches I_L/j, the top MOSFET enters Miller plateau. V_{dsi} decreases. The decreasing rate is governed by (14).

Stage 4: current ringing stage ($> t_4$).

After the MOSFET is on, the channel resistance is R_{on}. V_{dsi} is very small due to the small R_{on} of SiC MOSFET. Fig. 7 (b) shows the time-domain equivalent circuit.

The drain current overshoot during top switch turn-on transient is caused by the initial conditions and reverse recovery charge of the antiparallel diodes of the bottom switches. In the all-SiC power modules, the reverse recovery current is very small [28]. The magnitude of current oscillation largely depends on the initial conditions. Fig 7 (c) shows the equivalent frequency-domain circuit. Similarly, the initial voltage on the output capacitance of the bottom switch in the i^{th} HB is:

$$V_{ci2}(t_4) = V_{DC} - [i_{di}(t_4)(R_{di} + R_{on}) + i_{si}(t_4)R_{si} + i_C(t_4)ESR + V_{lead}(t_4) + V_{di} + V_{oi} + V_{si}] \tag{35}$$

where,

$$\begin{bmatrix} V_{di} \\ V_{oi} \\ V_{si} \end{bmatrix}_{t_4} = \boldsymbol{L_i} \cdot d \begin{bmatrix} i_{di}(t_4) \\ i_{di}(t_4) \\ i_{si}(t_4) \end{bmatrix} /dt + \boldsymbol{M_{i1}} \cdot d \begin{bmatrix} i_{d1}(t_4) \\ i_{d1}(t_4) \\ i_{s1}(t_4) \end{bmatrix} /dt + \ldots \boldsymbol{M_{ij}} d \begin{bmatrix} i_{di}(t_4) \\ i_{di}(t_4) \\ i_{si}(t_4) \end{bmatrix} /dt \quad (36)$$

The equivalent voltage sources are calculated by:

$$V_{1i} = \left(\left(\boldsymbol{L_i} \cdot \begin{bmatrix} i_{di}(t_4) \\ i_{di}(t_4) \\ i_{si}(t_4) \end{bmatrix} \right)^T + \left(\boldsymbol{M_{i1}} \cdot \begin{bmatrix} i_{d1}(t_4) \\ i_{d1}(t_4) \\ i_{s1}(t_4) \end{bmatrix} \right)^T + \cdots \left(\boldsymbol{M_{ij}} \cdot \begin{bmatrix} i_{di}(t_4) \\ i_{di}(t_4) \\ i_{si}(t_4) \end{bmatrix} \right)^T \right) \cdot \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} \quad (37)$$

$$V_{2i} = \left(\left(\boldsymbol{L_i} \cdot \begin{bmatrix} i_{di}(t_4) \\ i_{di}(4) \\ i_{si}(4) \end{bmatrix} \right)^T + \left(\boldsymbol{M_{i1}} \cdot \begin{bmatrix} i_{d1}(t_4) \\ i_{d1}(t_4) \\ i_{s1}(t_4) \end{bmatrix} \right)^T + \cdots \left(\boldsymbol{M_{ij}} \cdot \begin{bmatrix} i_{di}(t_4) \\ i_{di}(t_4) \\ i_{si}(t_4) \end{bmatrix} \right)^T \right) \cdot \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} + \frac{V_{ci2}(t_4)}{s} \quad (38)$$

$$V_{lead}(t_4) = (ESL + L_{lead}) \cdot \frac{di_C(t_4)}{dt} \quad (39)$$

$$i_C(t_4) = \sum_{i=1}^{j} i_{di}(t_4) \quad (40)$$

The voltages and currents can be solved from,

$$\begin{bmatrix} V_{ds12}(s) \\ \vdots \\ V_{dsj2}(s) \end{bmatrix} = \begin{bmatrix} V_{11} + V_{21} \\ \vdots \\ V_{1j} + V_{2j} \end{bmatrix} - \left(\begin{bmatrix} V_{d1}(s) + V_{o1}(s) + V_{s1}(s) \\ \vdots \\ V_{dj}(s) + V_{oj}(s) + V_{sj}(s) \end{bmatrix} - \begin{bmatrix} I_{d1}(s) \cdot (R_{d1} + R_{on1}) \\ \vdots \\ I_{dj}(s) \cdot (R_{dj} + R_{onj}) \end{bmatrix} - \begin{bmatrix} I_{s1}(s) \cdot R_{s1} \\ \vdots \\ I_{sj}(s) \cdot R_{sj} \end{bmatrix} - \begin{bmatrix} I_C(s) \cdot (s \cdot (ESL + L_{lead}) + ESR) \\ \vdots \\ I_C(s) \cdot (s \cdot (ESL + L_{lead}) + ESR) \end{bmatrix} \right) \quad (41)$$

where,

$$\begin{bmatrix} I_{s1}(s) \\ \vdots \\ I_{sj}(s) \end{bmatrix} = s \begin{bmatrix} C_{oss12} \cdot V_{ds12}(s) \\ \vdots \\ C_{ossj2} \cdot V_{dsj2}(s) \end{bmatrix} \quad (42)$$

$$\begin{bmatrix} V_{di}(s) \\ V_{oi}(s) \\ V_{si}(s) \end{bmatrix} = \boldsymbol{L_i} \cdot s \begin{bmatrix} I_{di}(s) \\ I_{di}(s) \\ I_{si}(s) \end{bmatrix} + \boldsymbol{M_{i1}} \cdot s \begin{bmatrix} I_{d1}(s) \\ I_{d1}(s) \\ I_{s1}(s) \end{bmatrix} + \ldots \boldsymbol{M_{ij}} \cdot s \begin{bmatrix} I_{dj}(s) \\ I_{dj}(s) \\ I_{sj}(s) \end{bmatrix} \quad (43)$$

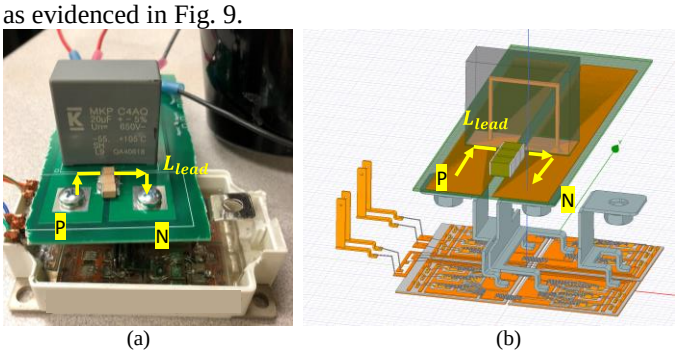
$$I_{DMij}(s) = \frac{V_{2j} - V_{2i}}{s(L_{si} + L_{sj} - 2M_{sisj}) + R_{sij} + \frac{1}{sC_{sij}}} + \frac{V_{1i} - V_{1j}}{sL_{dij} + s \cdot 2(M_{dij}) + R_{dij} + R_{oni} + R_{onj}} \quad (44)$$

$$I_{di}(s) = I_{DMij}(s) + I_{si}(s) \quad (45)$$

where $R_{sij} = R_{si} + R_{sj}$ and $C_{sij} = \frac{C_{ossi2} C_{ossj2}}{C_{ossi2} + C_{ossj2}}$.

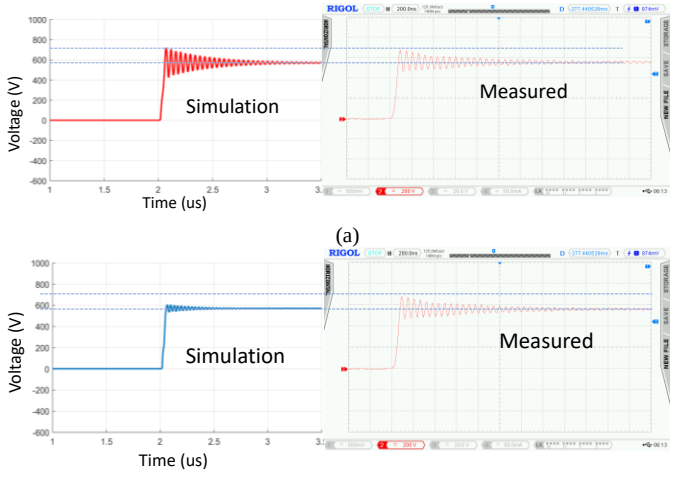
D. Discussion and model verification

Although the math model from (26) – (30) or (41) – (45) are very difficult to analytically solved, based on the model, the following important analysis and optimization can be conducted: 1) the proposed parasitic inductance model discloses that the switching transient of the power devices is not merely determined by the self-inductance and the mutual inductance within one HB as used in existing literatures, but rather by an inductance matrices which includes both self and mutual inductances of parallel branches; 2) the developed model discloses that the magnitudes of voltage and current ringing depend on the self-inductance of each HB branch, the mutual inductance between the HB branches and the ESL of the DC link capacitor because they determine the initial voltage sources; large self-inductance and positive mutual inductance lead to large initial voltage sources (note: *di/dt<0* in (22)); 3) based on (24) and (25), the SiC module layout can be optimized with negative mutual inductance to cancel the 1st term of the initial voltage equations, so the proposed layout technique generates negative mutual inductance to reduce initial values to reduce overshoot and ring magnitude; while most other papers focuses on reducing self-inductance within one HB; 4) based on the developed model, the overshoot and ring magnitude can be reduced by reducing both self and mutual inductance; 5) The proposed model gives more accurate voltage overshoot and ringing predictions because the mutual inductance is included as evidenced in Fig. 9.



(a) (b)

Fig. 8. The SiC power module with the external bus bar: (a) prototype and (b) 3D simulation model.



(a)

(b)

Fig. 9. Measured turn-off transient waveform compared with the simulated based on: (a) the proposed model (b) the model without mutual inductance.

In this paper, the parasitic inductance is extracted with Ansys Q3D in Fig. 8 (b). The maximum mutual inductance between L_{lead} and the CCL segments inside the module is 1.05 nH, much smaller than the self- inductance (around 20 nH) of each segment of the HB in (46) – (48). Therefore, it can be ignored. The assumption in Section II-B is thus valid.

To show the influence of mutual inductance, the self and mutual inductance matrices are extracted. The inductance matrices of the left two HBs in Fig. 2 are shown in (46) – (48),

$$\boldsymbol{L_1} = \begin{bmatrix} 20.73 & -1.22 & -6.12 \\ -1.22 & 21.61 & -4.17 \\ -6.12 & -4.17 & 19.59 \end{bmatrix} \text{nH} \quad (46)$$

$$\boldsymbol{L_2} = \begin{bmatrix} 20.3 & -1.01 & -6.05 \\ -1.01 & 21.58 & -4.19 \\ -6.05 & -4.19 & 19.1 \end{bmatrix} \text{nH} \quad (47)$$

$$\boldsymbol{M_{12}} = \begin{bmatrix} 17.74 & -0.93 & -6.1 \\ -1.02 & 9.49 & -4.14 \\ -6.07 & -4.97 & 17.61 \end{bmatrix} \text{nH} \quad (48)$$

(46) and (47) are the self-inductance matrices of HB 1 and 2, as defined in (2). (48) is the mutual inductance matrix, as defined in (3). The effects of P and N bus-bar terminals have been included in both self and mutual inductance matrices as all half-bridges share P and N bus-bar terminals. As mentioned, due to the small position angle between two HBs, the mutual inductances are large and positive.

In power modules with a phase leg configuration, the voltage and current oscillations can cause crosstalk. The crosstalk is caused by the capacitive and inductive couplings between the device gate loop and the power loop [28]. The switching of one switch can induce spurious gate voltage on the complementary switch. The capacitive coupling is through the device gate to drain capacitance. When the drain to source voltage changes, a current will be induced across the gate to drain capacitance, causing gate voltage variation. The inductive coupling is through the mutual inductance between the gate loop and the power loop. The current in the power loop induces a voltage in the device's gate loop. Both voltage and current oscillation contribute to the crosstalk. Serious crosstalk can lead to false turn-ons and the negative gate voltage breakdown.

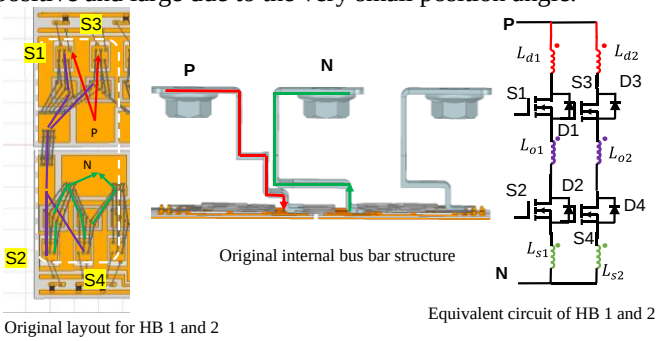
To validate the developed model, the self and mutual inductance matrices, as well as the L_{lead}, are extracted with Ansys Q3D. SiC MOSFETs and Schottky diodes are characterized using the Ansys Simplorer device characterization tool. Both static and dynamic characteristics are curvedly fitted based on the device datasheets. The drain-to-source voltage of the top SiC MOSFETs on the 1st HB is measured and simulated.

The measured and the simulated turn-off switching waveforms match very well in Fig.9 (a). On the other hand, the simulation results without the mutual inductance between two HBs in Fig. 9 (b) cannot match the measured. The measured turn-off overshoot voltage in Fig. 9 (a) is about 120 V, while the turn-off overshoot voltage in Fig. 9 (b) is about 70 V. With the proposed model, the transient analysis is much more accurate than the traditional model. The comparison also proves the significance of mutual inductance.

III. Layout Improvement

Based on the transient analysis in Section II, the magnitude of voltage and current ringing is determined by both the self and mutual inductance matrices. Therefore, the oscillations could be reduced through power module layout optimization. The layout optimization should not only focus on the reduction of the self-inductance, but also the mutual inductance. In self-inductance matrix $\boldsymbol{L_i}$, the self-inductance should be as small as possible, and the mutual inductance should be negative; the mutual inductance in $\boldsymbol{M_{ij}}$ between parallel HBs should be negative or small. Three techniques are used to achieve this. First, both the loop length and area of each HB should be as small as possible. Second, the position angle of corresponding current path segments in parallel HBs should be 180° to achieve negative mutual inductance. Third, the P-N HB loops should not be overlapped to reduce mutual inductance. In this paper, the DBC layout and the internal bus bar structure are improved.

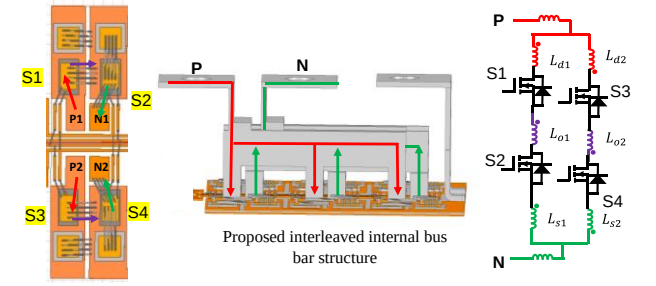
The layout of the two parallel HBs, internal bus bar structure and the equivalent circuit of HB 1 and 2 along with the current path segments and their associated parasitic inductances in the original and the proposed modules are shown in Figs.10 and 11 respectively. In the original layout in Fig. 11, the top and bottom switches are located in the top and bottom regions of the module; consequently, the current path loop area and the total self-inductance from P terminal to N terminal is large for each HB. At the same time, the current path segments share the same path on the internal bus bar. The mutual inductances between current path segments, such as L_{d1} and L_{d2} are, therefore positive and large due to the very small position angle.



Original layout for HB 1 and 2

Equivalent circuit of HB 1 and 2

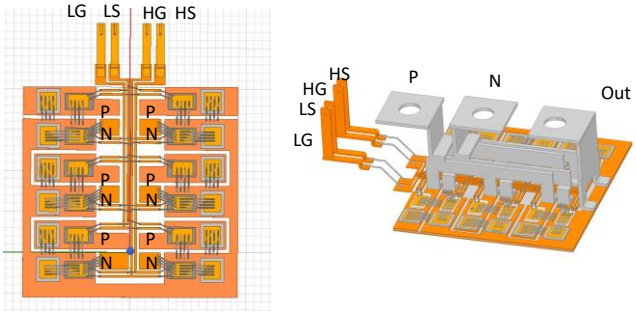
Fig. 10 The original module has large self and mutual inductances between two parallel HBs.



Proposed layout for HB 1 and 2

Equivalent circuit of HB 1 and 2

Fig. 11 The proposed module has small self and mutual inductances between two parallel HBs.



(a) (b)

Fig.12 (a) proposed layout design with terminals hidden and (b) proposed module design with terminals.

In the proposed layout in Fig. 11, the top and bottom switches are very close, so the P-to-N loop is small, and the inductance of every single HB is reduced. Meanwhile, the corresponding current path segments in two parallel HBs are separated and positioned at a 180° angle on the layout. The current path segments on the internal bus bar are also separated and interleaved. So, the mutual inductance between them is small.

As shown in Fig. 12, an HB multichip power module with the same power rating as the original commercial module is designed. The distances between parallel chips and between parallel HBs are determined by the heat dissipation angle [5] and power clearance distance IEC 60664-1. The minimum distance is determined by the larger distance of the two to avoid heat overlaps. Drivers are connected by kelvin connection. The internal bus bars are soldered on DBC copper, as in Fig. 12 (b). The terminal locations and layout are the same as the original.

The parasitic inductance matrices of the top two HBs in Fig. 12 (a) are shown as (49) – (51) in comparison to (46) – (48).

$$\boldsymbol{L_{1\_p}} = \begin{bmatrix} 13.25 & 0.01 & -7.16 \\ 0.01 & 1.60 & -0.22 \\ -7.16 & -0.22 & 13.98 \end{bmatrix} \text{nH} \quad (49)$$

$$\boldsymbol{L_{2\_p}} = \begin{bmatrix} 13.57 & -0.05 & -5.74 \\ -0.05 & 1.64 & -0.17 \\ -5.47 & -0.17 & 10.63 \end{bmatrix} \text{nH} \quad (50)$$

$$\boldsymbol{M_{12\_p}} = \begin{bmatrix} 3.41 & -0.22 & -4.17 \\ -0.02 & 0.01 & -0.2 \\ -3.75 & -0.01 & 2.02 \end{bmatrix} \text{nH} \quad (51)$$

Compared to (46) – (48), both self and mutual inductance are reduced. In (51), the mutual inductance M_{d1d2} and M_{s1s2} are greatly reduced compared with those in (48). They are still positive because they include the inductance of the shared P and N bus bar terminals. The comparison of the simulated drain-to-source voltage ringing of the MOSFET in the first HB (from the left) in a double pulse tester is shown in Fig.13. Due to the reduced parasitic inductance, the overshoot and oscillation are both significantly reduced.

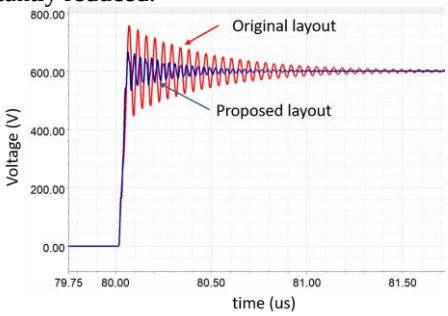


Fig.13 The comparison of the simulated drain-to-source voltage of the top switch during the turn-off transition between the original and proposed layouts.

The turn-off voltage overshoot and oscillation depend on the parasitic inductance not only inside but also outside the module. A parametric study was conducted on the proposed inductance model with L_{lead} increases from 0 nH to 30 nH. The simulated peak voltage overshoot in Fig. 14 shows that for the module under investigation, if L_{lead} is above 15 nH, the benefits of the minimized-inductance inside the module would be limited. Therefore, it is critical to minimize L_{lead} to fully take advantage of the proposed module layout. In this paper, paralleled DC link capacitors are used to minimize ESL and they are directly mounted to the terminals of the module, as a result, the measured total inductance L_{lead}+ESL is only 4.8 nH. Because of this, the module layout and internal bus bar optimization lead to a greatly reduced parasitic inductance.

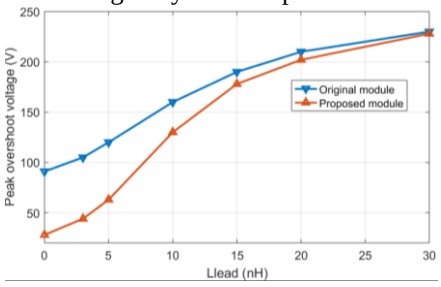


Fig.14 Simulated peak overshoot voltage comparison between the original module and the proposed module with different L_{lead}.

IV. Experimental Verification

An HB SiC multichip power module with the proposed layout was fabricated using wire bonds with a DBC process. The proposed module consists of 12 SiC MOSFETs (CPM2-1200-0025B) and 12 SiC Schottky diodes (CPW51200Z050B), the same as the commercial module. The fabricated prototype is shown in Fig.15. The self and mutual inductance of the original and proposed layouts are firstly extracted with S-parameter measurement. The transient responses of the two modules are tested with a double pulse tester.

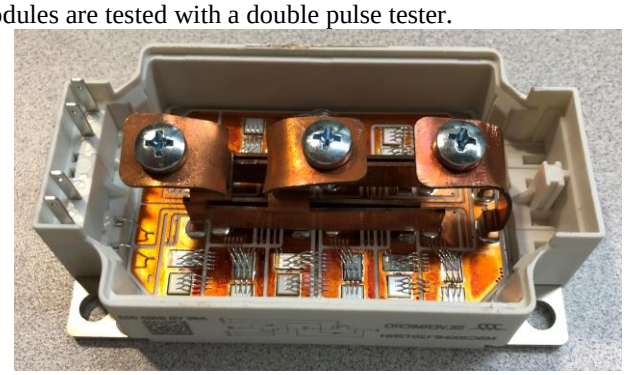


Fig.15 The prototype of the proposed HB SiC multichip power module.

A. Two-port S-parameters Measurement

Fig. 16 shows the extraction of self and mutual inductance of two inductors using S-parameters [24]. The inductance can be derived from the measured S-parameters in (52)-(56).

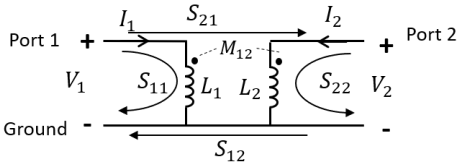
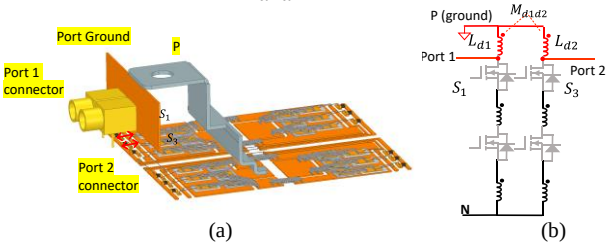


Fig. 16 Extraction of the inductance of two inductors with S-parameters.

For a pair of conductors with a common ground connection inside the power module, as in Fig. 17, port 1 and port 2 are connected to the DBC plane where the drains of the parallel MOSFETs S_1 and S_3 are positioned. The reference ground plane of the two ports is connected to the P terminal. Calibration was first conducted to the measurement interface, so the parasitics of the extra interconnections were excluded from the measurement results. The measured S-parameter matrix with PLANAR-808/1 network analyzer was converted to Z parameters based on (52) to (56). Self-inductance L_{d1}, L_{d2} and the mutual inductance M_{d1d2} are derived from (56).



(a) (b)

Fig. 17 Using two-port S-parameters to extract inductance with common ground connection: (a) ports and ground connections and (b) equivalent circuit.

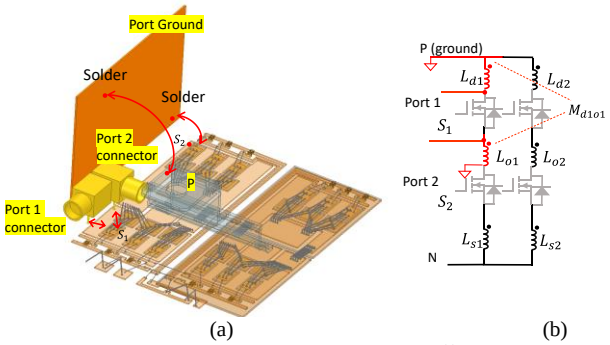
$$Z_{11} = Z_0 \frac{(1-S_{22})(1+S_{11})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \quad (52)$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \quad (53)$$

$$Z_{21} = Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \quad (54)$$

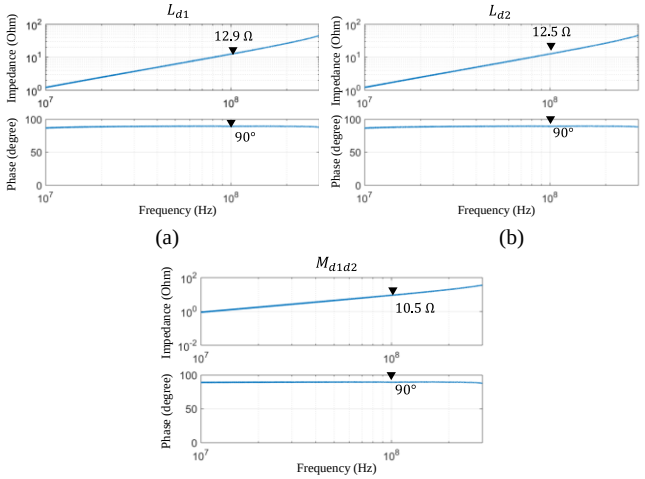
$$Z_{22} = Z_0 \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \quad (55)$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = j\omega \begin{bmatrix} L_{11} & M_{12} \\ M_{21} & L_{22} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (56)$$



(a) (b)

Fig. 18 Two-port S-parameters measurement with different ground connections: (a) ports and ground connections and (b) equivalent circuit.

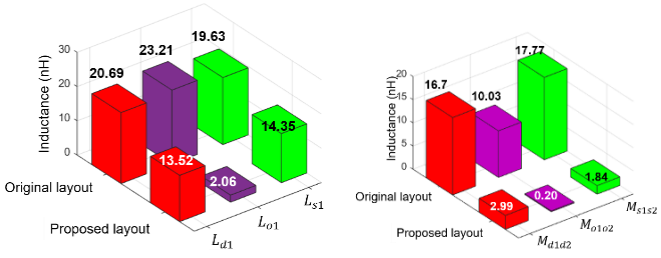


(a) (b)

(c)

Fig. 19 Extracted impedance: (a) L_{d1}, (b) L_{d2} and (c) M_{d1d2}.

If the conductors don't share the ground, one of the terminals of each conductor is locally connected to the reference ground of the two ports, as in Fig. 18. Port 1 is connected to the DBC plane where the drain of the MOSFET S_1 is positioned. Port 2 is connected to the source of the MOSFET S_1. The reference ground plane of the two ports is connected to the P terminal and the drain of S_2. This extracts the self-inductance L_{d1}, L_{o1} and the mutual inductance M_{d1o1}.



(a) (b)

Fig. 20. Comparison of the measured self and mutual inductance of the two modules: (a) self-inductance and (b) mutual inductance.

The extracted impedance curves are shown in Fig. 19. The extracted inductances for both the original and the proposed layouts are compared with the simulated in (46) - (48) and (49) - (51) in TABLE I and TABLE II. The simulated and the extracted match well.

The comparison of self and mutual inductance is shown in Fig. 20. Both self and mutual inductance are reduced.

TABLE I. INDUCTANCE OF THE ORIGINAL LAYOUT

(nH)	Simulated	Measured		Simulated	Measured
L_{d1}	20.73	20.69	M_{o2s2}	-4.19	-4.91
L_{d2}	20.30	19.89	M_{d1d2}	17.74	16.7
L_{o1}	21.61	23.21	M_{d1o2}	-0.93	-1.50
L_{o2}	21.58	23.17	M_{d1s2}	-6.10	-6.41
L_{s1}	19.59	19.63	M_{o1d2}	-1.02	-1.80
L_{s2}	19.10	19.22	M_{o1o2}	9.49	10.03
M_{d1o1}	-1.22	-2.34	M_{o1s2}	-4.14	-4.75
M_{d1s1}	-6.12	-6.32	M_{s1d2}	-6.07	-6.61
M_{o1s1}	-4.17	-4.97	M_{s1o2}	-4.97	-5.52
M_{d2o2}	-1.01	-2.09	M_{s1s2}	17.61	17.77
M_{d2s2}	-6.05	-6.33			

TABLE II. INDUCTANCE OF THE PROPOSED LAYOUT

(nH)	Simulated	Measured		Simulated	Measured
L_{d1}	13.25	13.52	M_{o2s2}	-0.03	-0.31
L_{d2}	13.57	13.8	M_{d1d2}	3.41	2.99
L_{o1}	1.60	2.06	M_{d1o2}	-0.22	-0.52
L_{o2}	1.64	1.82	M_{d1s2}	-4.17	-3.87
L_{s1}	13.98	14.35	M_{o1d2}	-0.02	-0.43
L_{s2}	14.22	14.59	M_{o1o2}	0.01	0.20
M_{d1o1}	0.01	0.47	M_{o1s2}	-0.01	0.20
M_{d1s1}	-7.16	-6.50	M_{s1d2}	-3.75	-3.29
M_{o1s1}	-0.22	-0.52	M_{s1o2}	-0.20	-0.20
M_{d2o2}	-0.05	-0.08	M_{s1s2}	2.02	1.84
M_{d2s2}	-7.47	-6.12			

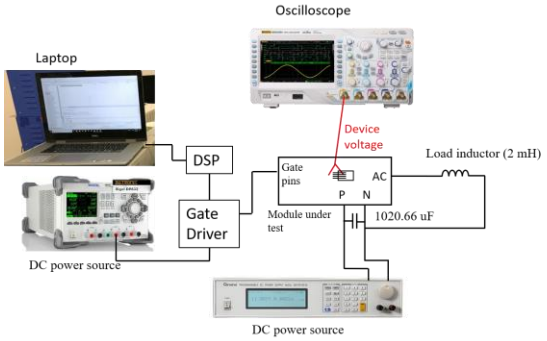
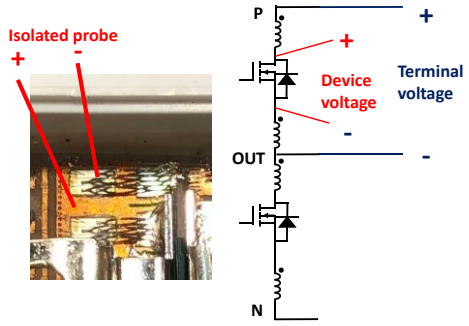


Fig. 21 Double pulse test setup.

B. Double Pulse Testing

The setup of a double pulse testing is shown in Fig. 21. The top switches are driven with a double pulse signal while the bottom switches are kept off. The gate resistors used in the experiments are 5.6 Ω. The DC link capacitors include a 0.97 mF electrolytic capacitor (Cornell Dubilier 947D), a 20 μF film capacitor (B32758G8306K000), and three 220nF ceramic capacitors (2220Y1K20224KXTWS3) in parallel. The load inductor is a 2 mH air-core inductor. The device voltage was measured by inserting the voltage probes into the insulating gel inside the power module as in Fig. 22 (a). The die voltage instead of terminal voltage can be measured in Fig. 22 (b).

The measured switching waveforms of the proposed and original layouts during the turn-off transition are shown in Fig. 23 at 600 V/120 A. The original layout has a peak overshoot of 120 V compared with 50 V of the proposed layout. The waveforms in Fig. 23 also match the simulation results in Fig.13. It is expected that the HF EMI caused by the voltage oscillation can be significantly reduced. The experimental results validate the effect of parasitic inductance reduction.



(a) (b)

Fig.22 a) drain-to-source voltage measurement, b) circuit.

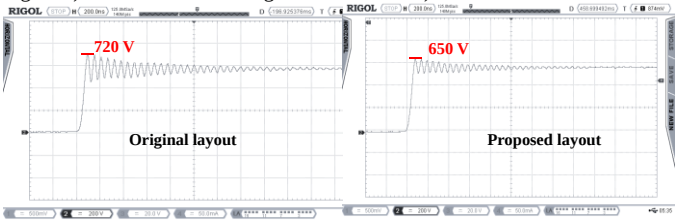
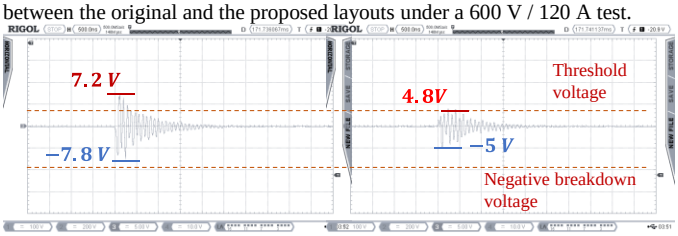
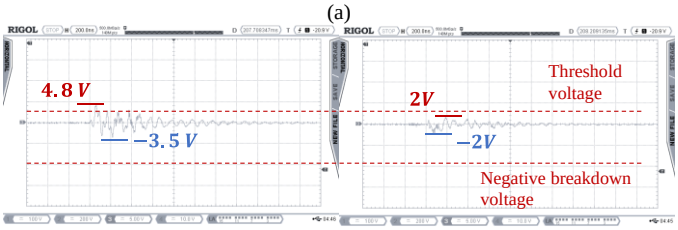


Fig.23. Comparison of the measured turn-off transient voltage waveforms between the original and the proposed layouts under a 600 V / 120 A test.



(a)



(b)

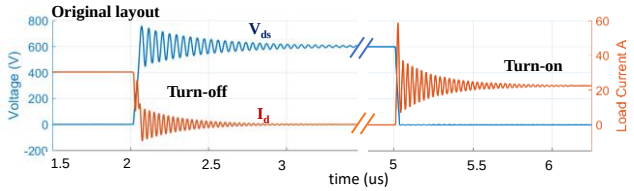
Fig. 24 Comparison of the measured gate voltage waveforms of the bottom switch when the top switch (a) turns on and (b) turns off.

The gate voltages of the bottom switches of the two modules are measured. Fig. 24 shows the measured gate voltage of the bottom switches during the top switch's switching transients. In the original module, the peak positive induced gate voltage is 7.2 V, higher than the threshold voltage (3V). The devices are falsely turn-on. The lowest negative induced voltage of the original layout is -7.8 V, close to the negative gate breakdown voltage (-10V). The off-state voltage of the driver cannot move to negative to avoid the false turn-on without risking device negative gate breakdown. In the proposed layout, due to the reduced parasitic inductance, the voltage and current oscillations, and the induced gate voltage is reduced. The highest and lowest induced gate voltages are 4.8 V and -5 V. Setting the off-state voltage to -4V can avoid the false turn-on. This greatly improves the reliability of the module [28].

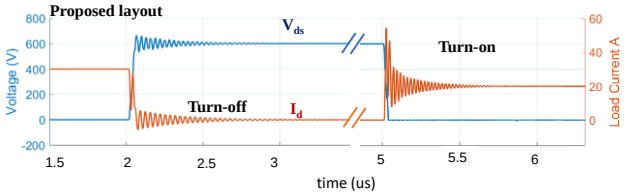
V. Thermal Consideration

To validate the proposed layout has no thermal issues. A thermal 3D FEA simulation was carried out in Ansys Icepak for both modules with an identical heatsink. The two modules are first simulated in Ansys Simplorer under 600V/120A at 70 kHz.

Based on the simulated V_{ds} and I_d in Fig. 25, the voltage and current ringings in the proposed module are smaller than the original module. As a result, the switching power loss of the proposed layout is 56 W vs. 67 W of the original layout. The conduction power loss of SiC MOSFET and diode is 2.4W and 16W for both cases. Three mesh levels were assigned. The maximum cubical mesh size for the DBC dies, and bus bars is 1 mm × 1 mm × 0.2 mm. The maximum mesh size for the region enclosing the module is 2 mm × 2 mm × 1 mm. The region outside the module is 5 times larger than the module dimensions in xyz directions. It is in an open region with 5 m/s air flow. The maximum mesh size of the air is 10 mm × 10 mm × 8 mm. The boundary of the region is opening. Gravity is 9.8 m/s^2.



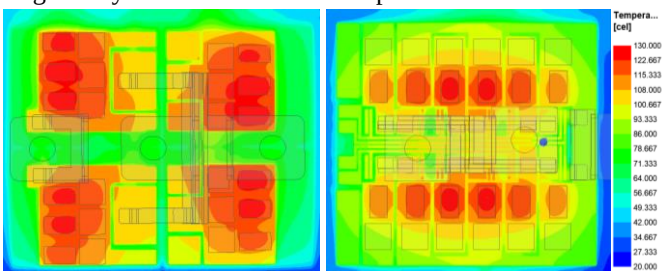
(a)



(b)

Fig. 25. Simulated switching waveforms during turn-on and turn-off transient for switching loss calculation: (a) Original layout (b) proposed layout.

The simulated results in Fig. 26 show that due to the reduced switching power loss, the highest junction temperature of the proposed layout is 120 ℃ which is lower than 130 ℃ of the original layout. The better thermal performance was achieved.



(a) (b)

Fig. 26. Simulated temperatures of (a) original layout and (b) proposed layout.

VI. Conclusions

Different from the conventional approaches, in this paper, the parasitic mutual inductance between parallel current path segments are included in the parasitic inductance model of SiC multichip power modules. The mutual inductance plays an important role in the voltage ringing during switching transients. The ring can be reduced with negative mutual inductance which can be realized with a 180° position angle between parallel current path segments. The parasitic inductance extracted with the proposed technique matches the simulated well. A novel layout was proposed to reduce the parasitic inductance. Double-pulse testing and thermal

simulations validated that the proposed technique can reduce voltage ringing, crosstalk effect, power loss, and thermal stress.

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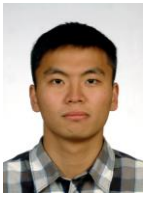

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