Develop Parasitic Inductance Model for the Planar Busbar of an IGBT H Bridge in a Power Inverter

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***Abstract*—This paper first analyzes the current paths on a planar busbar based on insulated-gate bipolar transistor bridge switching states and dc-link capacitor configurations. The busbar's circuit models which include both self- and mutual inductances are developed based on the identified current paths. The inductance circuit models are analyzed and reduced for different switching states, transition states, and dc-link capacitor configurations. Inductance and current sharing is analyzed based on circuit theory. Both simulations and measurements are conducted to verify the developed technique.**

***Index Terms*—Current path, dc-link capacitor, insulated-gate bipolar transistor (IGBT) bridge, loop inductance, mutual inductance, partial inductance, planar busbar, self-inductance.**

I. Introduction

THE inductances of the planar dc busbar of an insulated-gate bipolar transistor (IGBT) inverter play an important role in the switching operation of inverter [11], [12]. Because of the fast switching of IGBT, high *di/dt* results in high voltage drops on the inductances and at the same time, the inductances resonate with the junction capacitance or snubber capacitors of IGBTs [4]. It causes high voltage spikes which may kill IGBTs [1]. The high voltage spikes also generate electromagnetic interference (EMI) and directly increase IGBT's power losses [2]. Low busbar inductances are therefore preferred. Because of this, the analysis, extraction, and measurement of the inductances for a planar busbar are very important for the design and evaluation of a busbar.

Papers [3], [10], [14] propose a method to model the inductances and resistances of a busbar by decomposing the busbar into numerous elementary LR segments based on the physical dimensions and structures of the busbar. Paper [4] investigates the effects of busbar inductances on IGBT voltage spikes. Paper [5] calculates busbar inductances-based time-domain waveforms. Paper [7] simulates the inductances using an electromagnetic simulation tool. Paper [8] explores a method for inductance extraction based on current commutation loops and FEA. Paper [9] presents a method using time-domain reflectometry to extract busbar inductance.

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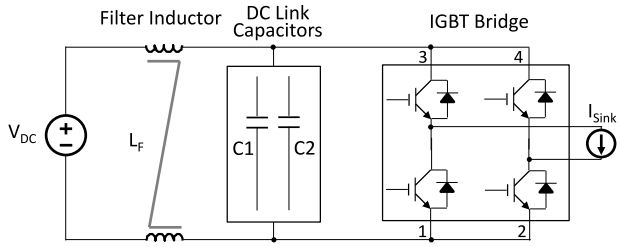

Fig. 1. Circuit of an inverter system under investigation.

Different from existing literatures, this paper develops parasitic self- and mutual inductance circuit models based on the fact that the current paths are a function of IGBT bridge switching states, dc-link capacitor structures, and the connections of dc-link capacitor, IGBT and filter inductors. In Section II, this paper will first analyze the current paths and inductance circuit model for the planar busbar of an IGBT H Bridge. The inductance and current sharing is investigated in Section III. The inductance matrices are extracted with electromagnetic simulation tool in Section IV. The loop inductance is calculated based on the extracted inductance matrices and developed formulas. Busbar current distributions for two dc-link capacitor configurations are analyzed, simulated, and compared. Measurement verification is presented in Section V. The capacitance of the planar busbar will not be investigated in this paper.

II. Current Paths and Inductance Model of a Planar Busbar

This section first analyzes the current paths on a planar busbar in a single-phase inverter. Effects of dc-link capacitor's configuration on the current paths between IGBTs and dc-link capacitors will be analyzed. Based on the analysis, the inductance circuit models are developed for the busbar.

A. Current Paths on a Planar Busbar

Fig. 1 shows the circuit of an inverter system to be investigated. Fig. 2(a) shows the three-layer aluminum busbar prototype under investigation. The dimensions of top or bottom busbar plate are 105.5 mm $\times$ 219.50 mm $\times$ 1.5 mm. Fig. 2(b) shows a popular connection of the planar busbar, dc-link capacitors, and an IGBT bridge module in practice.

In Fig. 1, the dc source feeds the power to the IGBT bridge through an *LC* low-pass filter. In an actual design in Fig. 2(a) and (b), the filter inductor L_F and dc source $V_{\rm DC}$ are connected from outside of the planar busbar to the terminals S1 and S2 of the busbar. IGBT bridge module is mounted under the planar busbar. As shown in Fig. 2(b), IGBT terminals 1 and 2 are connected to the bottom plate of the busbar. Terminals 3 and 4 are connected

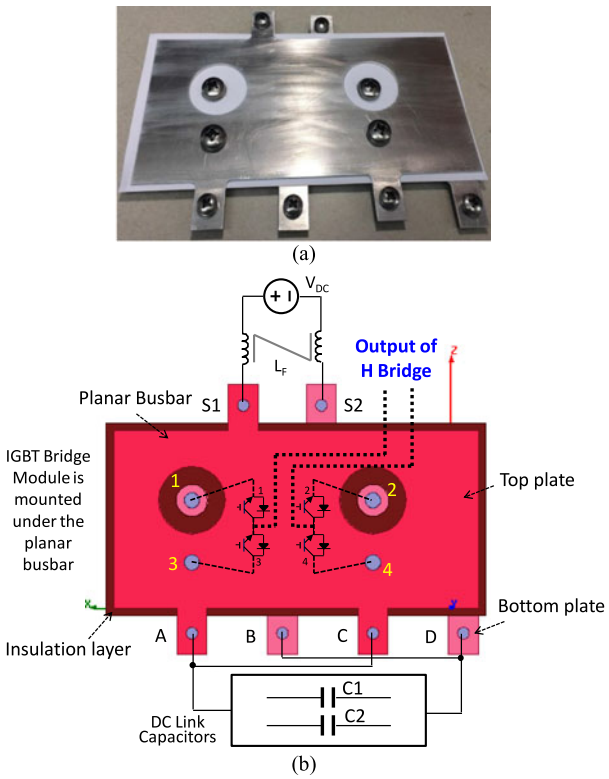

Fig. 2. IGBT planar busbar: (a) prototype under investigation and (b) electrical connections between the busbar and dc-link capacitors, and between an IGBT H bridge module and a filter inductor.

to the top plate of the busbar. It should be pointed out that the IGBT bridge in Fig. 2(b) is upside down compared with that in Fig. 1. The outputs of the IGBT bridge are routed under the planar busbar to the same side of the dc inputs as shown by the thick dash lines in Fig. 2(b). It should be noted that the current paths represented by the thick dash lines are not on the busbar under investigation. They are on a separated busbar which is connected to an inverter load. An insulation layer is laminated between the bottom and top plates. The dc-link capacitors are connected to A, C tabs on the top plate and B, D tabs on the bottom plate. The dc-link capacitors in the practical design in Fig. 2(b) are therefore on a different side of the IGBT bridge from that in the circuit of Fig. 1. This busbar structure is one of the most popular industry designs as it is easy to physically layout the dc-bus inputs and inverter outputs on the same side of the inverter box. It offers a convenient electrical interface. Because of this, it is meaningful to analyze this structure in this paper.

In Fig. 2(b), the ac current distribution inside the busbar is uneven not only because of skin and proximity effects but also because of the impedance difference of current paths between IGBT terminals and capacitor tabs. The impedances of current paths are a function of electrical connections. For example, the impedances between IGBT terminal 3 and capacitor tab A is different from that between IGBT terminal 3 and tab C. Furthermore, the current paths are also a function of IGBT bridge switching states. Because of this, the inductance of the busbar should be analyzed based on both electrical connections and IGBT bridge's switching states.

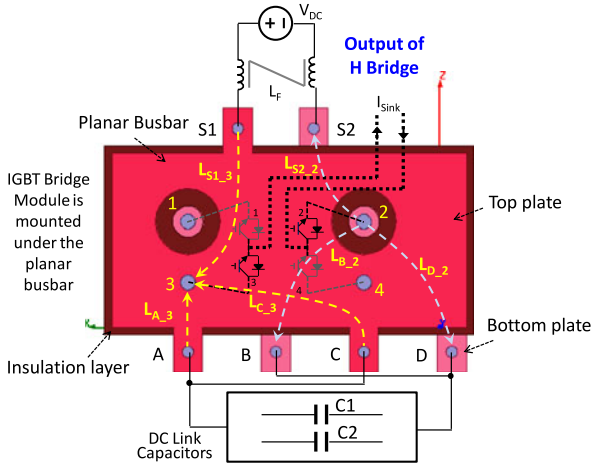

Fig. 3. Current paths on the planar busbar at state 10.

Because the output of the inverter is either connected to an inductive electrical machine in a motor drive system or a coupling inductor in a grid-connected inverter system, it is assumed that the load is a current sink I_{Sink}. Furthermore, because filter inductance L_F is designed to filter out switching ripples, it has high impedance to switching current ripples. Its impedance is much larger than those of any inductances of the busbar so V_{DC} and L_F can be considered as a dc current source at steady state in the concerned frequency range.

In Fig. 1, the IGBT bridge has four switching states: 00, 01, 10, and 11. Switching state 00 is the state when the bottom switches of both legs turn on so the output voltages of both legs are equal to 0 V. Switching state 01 is the state when the bottom switch of the left leg and the top switch of the right leg turn on so the output voltage of the left leg is 0 V and the output voltage of the right leg is equal to the dc-bus voltage. Switching state 10 is the state when the top switch of the left leg and the bottom switch of the right leg turn on so the output voltage of the left leg is equal to the dc-bus voltage and the output voltage of the right leg is 0 V. Switching state 11 is the state when the top switches of both legs turn on so the output voltages of both legs are equal to the dc-bus voltage. There are also transition states between two switching states.

At state 10, the top switch of the left leg and the bottom switch of the right leg conduct currents. Because the actual IGBT connections in Fig. 2(b) are upside down compared with the circuit in Fig. 1, the current paths are illustrated in Fig. 3 in detail based on the practical connections. In Fig. 3, each current path is represented with its self-inductance. On the top plate of the busbar, the currents flow from the dc source via current path L_{S1_3} and the dc-link capacitors via current paths L_{A_3} and L_{C_3} into the terminal 3 of the left leg of the IGBT bridge. The currents flow out from the left leg of the bridge to the load of the inverter and flow back to the right leg of the bridge. The currents finally flow out from terminal 2 on the right leg of IGBT bridge to dc source via current paths L_{S2_2} and the dc-link capacitors via current paths L_{B_2} and L_{D_2} on the bottom plate of the busbar. So, there are two current paths L_{B_2} and L_{D_2} from IGBT bridge terminal 2 to dc-link capacitors and two current paths L_{A_3} and L_{C_3} from dc-link capacitors to IGBT bridge

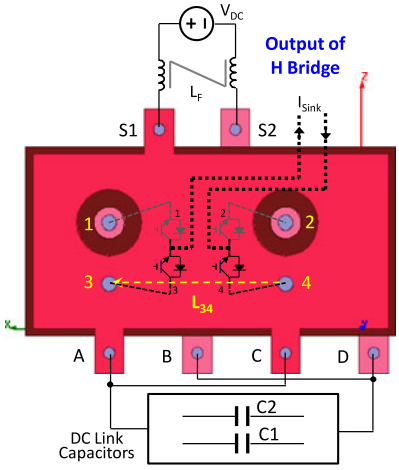

Fig. 4. Current paths on the planar busbar at state 11.

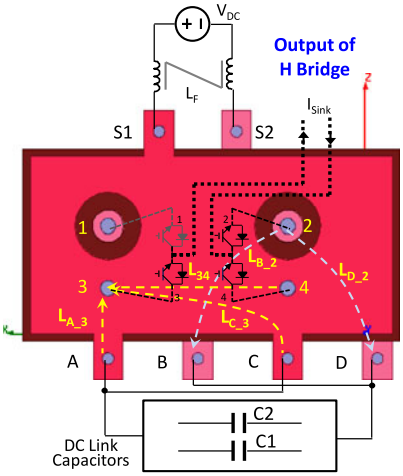

Fig. 5. Current paths on the planar busbar during the transition from states 10 to 11.

terminal 3. As analyzed previously, $V_{\rm DC}$ and L_F are like a dc current source, so $V_{\rm DC}$ and L_F, busbar inductances L_{S1_3} and L_{S2_2} and their mutual inductances will be removed in later analysis.

The dc-link capacitor loop is composed of the IGBT bridge, busbar self-inductances L_{A_3}, L_{C_3}, L_{B_2}, L_{D_2} and dc-link capacitors. There is a mutual inductance between any two of the self-inductances.

The current path at switching state 11 is shown in Fig. 4. The load current $I_{\rm Sink}$ flows from IGBT terminals 4 to 3 via the top plate of the busbar. For switching states 00 and 01, the current paths can be analyzed similarly.

During the transition from states 10 to 11, the load current $I_{\rm Sink}$ charges the junction capacitance or snubber capacitors of the two IGBTs in the right leg in Fig. 1. Therefore, there are currents flowing through both top and bottom switches of the right leg. The current flows out from IGBT terminals 2 and 4, and then flows back to terminal 3 via busbar and dc-link capacitors. The current paths are shown in Fig. 5.

There is a mutual inductance between any two of the self-inductances in Fig. 5.

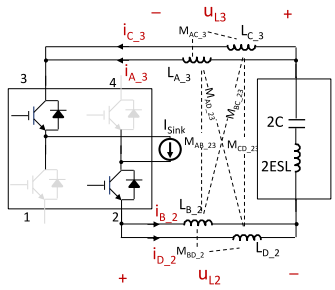

Fig. 6. Equivalent circuit at state 10 when two dc-link capacitors are paralleled.

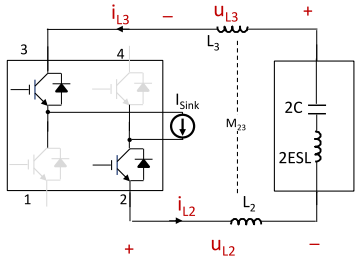

Fig. 7. Reduced equivalent circuit at state 10 when two dc-link capacitors are paralleled.

Other current paths during transitions can be analyzed in the same way as above.

B. Inductance Model of a Planar Busbar

In Fig. 1, the two dc-link capacitors could have two configurations. For the first configuration, the two capacitors are paralleled inside the package. It is like one capacitor. For the second configuration, the two dc-link capacitors are separated. So, it is like two capacitors. The inductance circuit models are different for these two configurations. The equivalent series inductances (ESL) of dc-link capacitors are included in the discussion in this paper.

1) Two DC-Link Capacitors Are Paralleled: When two dc-link capacitors are paralleled in capacitor package, they are like one capacitor. At switching state 10, Fig. 3 can be represented with the equivalent circuit in Fig. 6.

The mutual inductance between any two of the self-inductances on the busbar is shown in Fig. 6. In Fig. 6, L_{A_3} and L_{C_3} are in parallel; L_{B_2} and L_{D_2} are in parallel. Because of this, L_{A_3}, L_{C_3}, L_{B_2}, L_{D_2} and their mutual inductances in Fig. 6 can be equivalently represented with the L_3, L_2, and M_{23} in Fig. 7. M_{23} is the mutual inductance between L_2 and L_3. L_2, L_3, and M_{23} will be derived in Section III.

Fig. 7 shows the reduced equivalent circuit. L_2, L_3, and M_{23} can be further equivalent to an inductance equal to $L_2+L_3+2M_{23}$ if necessary.

The equivalent circuit of switching state 01 can be analyzed in the same way as above.

When IGBT bridge is at switching state 11, Fig. 4 can be represented with the equivalent circuit in Fig. 8. The load current $I_{\rm Sink}$ flows from IGBT bridge terminals 4 to 3 via busbar inductance L_{34}. The equivalent circuit of switching states 00 can be analyzed in the same way as that in Fig. 8.

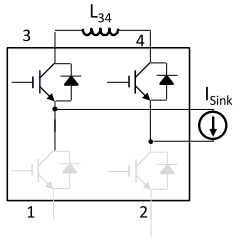

Fig. 8. Equivalent circuit at state 11 when two dc-link capacitors are paralleled.

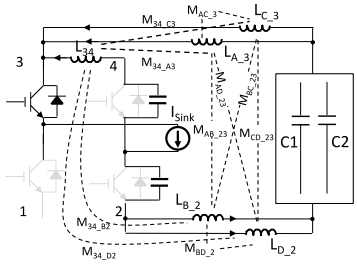

Fig. 9. Equivalent circuit during the transition from states 10 to 11 when two dc-link capacitors are paralleled.

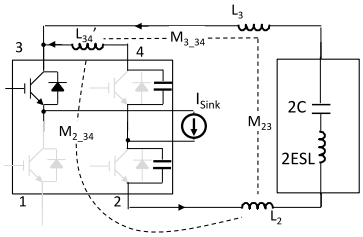

Fig. 10. Reduced equivalent circuit during the transition from states 10 to 11 when two dc-link capacitors are paralleled.

During the transition from states 10 to 11, the current paths in Fig. 5 can be represented with the equivalent circuit in Fig. 9. The mutual inductances between any two of the self-inductances are shown in Fig. 9. Fig. 9 can be reduced to Fig. 10. L_2, L_3, and M_{23} are different from those in Fig. 7 as they are incorporated with the effects of the mutual couplings to L'_{34}.

2) Two DC-Link Capacitors Are Separated: When two separate dc-link capacitors are connected to the planar busbar, the current paths for switching state 10 are shown in Fig. 11. It is assumed that capacitor C_1 is connected to tabs AB and capacitor 2 is connected to tabs CD. Each current path has a self-inductance. There is a mutual inductance between any two self-inductances. Fig. 12 shows the equivalent circuit model.

In Fig. 12, L_{C_3} and L_{D_2} with mutual inductance M_{CD_23} are on the same current path. L_{A_3} and L_{B_2} with mutual inductance M_{AB_23} are on the same current path. All other mutual inductances are between the two current paths. Because of this, Fig. 12 can be further reduced to Fig. 13.

L_{C_3}, L_{D_2}, and M_{CD_23} in Fig. 12 can be equivalent to L_{CD_23} in Fig. 13. Similarly, L_{A_3}, L_{B_2}, and M_{AB_23} can be equivalent to L_{AB_23}. Effects of all other mutual inductances between the two current paths are represented with M_{23}.

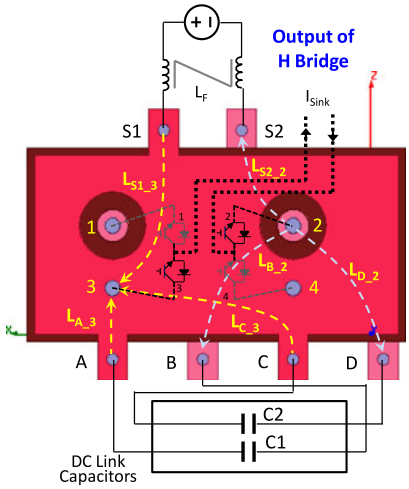

Fig. 11. Current paths on the planar busbar at state 10 when two dc-link capacitors are separated.

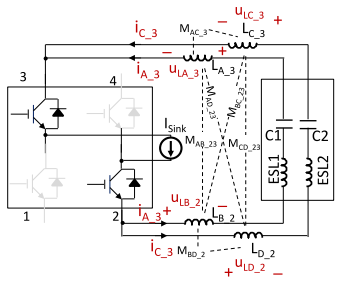

Fig. 12. Equivalent circuit at state 10 when two dc-link capacitors are separated.

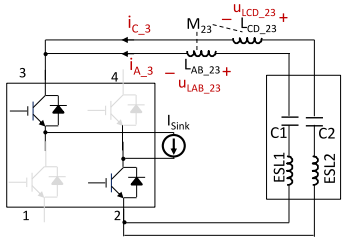

Fig. 13. Reduced equivalent circuit when two dc-link capacitors are separated.

The equivalent circuit for switching states 01 can be analyzed in the same way as above. The equivalent circuit for the switching states 00 and 11 can be derived similarly to that in Fig. 8.

During the transition from states 10 to 11, the current paths are shown in Fig. 14 and the reduced equivalent circuit can be represented with Fig. 15. L_{CD_23}, L_{AB_23}, and M_{23} are different from those in Fig. 13 as they are incorporated with the effects of mutual couplings to L_{34}'.

During other transitions, the equivalent circuits can be derived similarly.

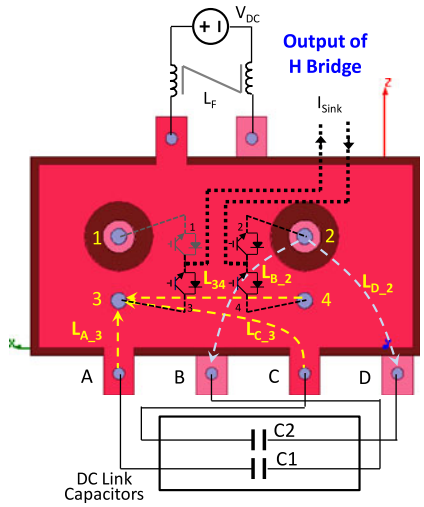

Fig. 14. Current paths on the planar busbar during the transition from states 10 to 11 when two dc-link capacitors are separated.

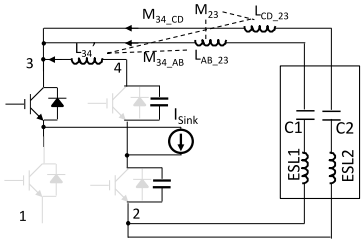

Fig. 15. Reduced equivalent circuit during the transition from states 10 to 11 when two dc-link capacitors are separated.

III. Analysis of Inductance and Current Sharing of Current Paths

A. Busbar Model When Two DC-link Capacitors Are Paralleled

It has been analyzed in Section II that when the two dc-link capacitors are paralleled, at state 10, the equivalent circuit in Fig. 6 can be reduced to that in Fig. 7. L_2, L_3, and M_{23} in Fig. 7 can be determined based on the self- and mutual inductances in Fig. 6. In Fig. 6, the voltages u_{L3} and u_{L2} across inductances, the currents i_{A_3}, i_{C_3}, i_{B_2}, and i_{D_2} flowing through the inductances and all the self- and mutual inductances should meet the condition in (1) in s domain

$$\begin{bmatrix} u_{L3} \\ u_{L3} \\ u_{L2} \\ u_{L2} \end{bmatrix} = s \begin{bmatrix} L_{C\_3} & M_{AC\_3} & M_{BC\_23} & M_{CD\_23} \\ M_{AC\_3} & L_{A\_3} & M_{AB\_23} & M_{AD\_23} \\ M_{BC\_23} & M_{AB\_23} & L_{B\_2} & M_{BD\_2} \\ M_{CD\_23} & M_{AD\_23} & M_{BD\_2} & L_{D\_2} \end{bmatrix} \begin{bmatrix} i_{C\_3} \\ i_{A\_3} \\ i_{B\_2} \\ i_{D\_2} \end{bmatrix} = sL \begin{bmatrix} i_{C\_3} \\ i_{A\_3} \\ i_{B\_2} \\ i_{D\_2} \end{bmatrix} \tag{1}$$

where L represents the 4×4 inductance matrix. The currents i_{L3} and i_{L2} are equal in Fig. 7. The currents in Figs. 6 and 7 meet the condition described in

$$\begin{bmatrix} i_{L3} \\ i_{L2} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_{C\_3} \\ i_{A\_3} \\ i_{B\_2} \\ i_{D\_2} \end{bmatrix}. \tag{2}$$

The voltages, currents, self-inductances, and mutual inductances in Fig. 7 meet the conditions in

$$\begin{bmatrix} u_{L3} \\ u_{L2} \end{bmatrix} = s \begin{bmatrix} L_3 & M_{23} \\ M_{23} & L_2 \end{bmatrix} \begin{bmatrix} i_{L3} \\ i_{L2} \end{bmatrix}. \tag{3}$$

Based on (1) to (3), the self-inductances L_2, L_3 and the mutual inductance M_{23} in Fig. 7 can be derived in

$$\begin{bmatrix} L_3 & M_{23} \\ M_{23} & L_2 \end{bmatrix} = \left(\begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} L^{-1} \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{bmatrix} \right)^{-1}. \tag{4}$$

The currents flowing through L_{A_3}, L_{C_3}, L_{B_2}, and L_{D_2} can be derived based on (1)–(3) in

$$\begin{bmatrix} i_{C\_3} \\ i_{A\_3} \\ i_{B\_2} \\ i_{D\_2} \end{bmatrix} = L^{-1} \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 \end{bmatrix} L^{-1} \begin{bmatrix} i_{L3} \\ i_{L3} \\ i_{L2} \\ i_{L2} \end{bmatrix}. \tag{5}$$

The current sharing within two parallel current paths in Fig. 6 can be analyzed with (5). From (5), the currents are the function of all self- and mutual inductances. However, if the self-inductances are much larger than the mutual inductances, the currents inside the inductances are mainly determined by the self-inductances

$$\frac{i_{C\_3}}{i_{A\_3}} = \frac{L_{A\_3}}{L_{C\_3}}; \frac{i_{B\_3}}{i_{D\_3}} = \frac{L_{D\_3}}{L_{B\_3}}. \tag{6}$$

From (6), more current will flow through the lower inductance of the two.

During the transition from states 10 to 11, the equivalent circuit in Fig. 9 can be reduced to that in Fig. 10. The self- and mutual inductances in Fig. 10 can be derived based on Fig. 9. Following the same procedure as used from (1) to (4), the self-inductances L_2, L_3, L'_{34} and the mutual inductances M_{23}, M_{2_34}, and M_{3_34} can be derived as (7).

As stated previously, L_2, L_3, and M_{23} are different from those in (4) since they are incorporated with the effects of mutual couplings to L_{34}'

$$\begin{bmatrix} L_3 & M_{23} & M_{3\_34} \\ M_{23} & L_2 & M_{2\_34} \\ M_{3\_34} & M_{2\_34} & L'_{34} \end{bmatrix}$$

$$= \left(\begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \right.$$

$$\begin{bmatrix} L_{C\_3} & M_{AC\_3} & M_{BC\_23} & M_{CD\_23} & M_{34\_C3} \\ M_{AC\_3} & L_{A\_3} & M_{AB\_23} & M_{AD\_23} & M_{34\_A3} \\ M_{BC\_23} & M_{AB\_23} & L_{B\_2} & M_{BD\_2} & M_{34\_B2} \\ M_{CD\_23} & M_{AD\_23} & M_{BD\_2} & L_{D\_2} & M_{34\_D2} \\ M_{34\_C3} & M_{34\_A3} & M_{34\_B2} & M_{34\_D2} & L_{34} \end{bmatrix}^{-1}$$

$$\left. \begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \right)^{-1} . \tag{7}$$

The current sharing is not derived since during the transition, the current commutates to L_{34} quickly.

The accuracy of the calculated self- and mutual inductances depends on the accuracy of the extracted inductance matrix as (7) is derived rigorously.

B. Busbar Model When Two DC-Link Capacitors Are Separated

It has been analyzed in Section II that when the two dc-link capacitors are separated, the equivalent circuit in Fig. 12 can be reduced to the circuit in Fig. 13. L_{CD_23}, L_{AB_23}, and M_{23} in Fig. 13 can be determined based on the self- and mutual inductances in Fig. 12. In Fig. 12, the voltages u_{LC_3}, u_{LA_3}, u_{LB_2}, and u_{LD_2} across inductances, the currents i_{C_3} and i_{A_3} flowing through the inductances and all the self- and mutual inductances should meet the condition defined in (8) in *s* domain

$$\begin{bmatrix} u_{LC\_3} \\ u_{LA\_3} \\ u_{LB\_2} \\ u_{LD\_2} \end{bmatrix} = s \begin{bmatrix} L_{C\_3} & M_{AC\_3} & M_{BC\_23} & M_{CD\_23} \\ M_{AC\_3} & L_{A\_3} & M_{AB\_23} & M_{AD\_23} \\ M_{BC\_23} & M_{AB\_23} & L_{B\_2} & M_{BD\_2} \\ M_{CD\_23} & M_{AD\_23} & M_{BD\_2} & L_{D\_2} \end{bmatrix} \begin{bmatrix} i_{C\_3} \\ i_{A\_3} \\ i_{A\_3} \\ i_{C\_3} \end{bmatrix}$$

$$= sL \begin{bmatrix} i_{C\_3} \\ i_{A\_3} \\ i_{A\_3} \\ i_{C\_3} \end{bmatrix} . \tag{8}$$

In (8), L represents the 4×4 inductance matrix. The voltage u_{LCD_23} and u_{LAB_23} in Fig. 13 and the inductance voltages in Fig. 12 meet the condition described in

$$\begin{bmatrix} u_{LCD\_23} \\ u_{LAB\_23} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} u_{LC\_3} \\ u_{LA\_3} \\ u_{LB\_2} \\ u_{LD\_2} \end{bmatrix} . \tag{9}$$

The voltages, currents, self- and mutual inductances in Fig. 13 meet the conditions in

$$\begin{bmatrix} u_{LCD\_23} \\ u_{LAB\_23} \end{bmatrix} = s \begin{bmatrix} L_{CD\_23} & M_{23} \\ M_{23} & L_{AB\_23} \end{bmatrix} \begin{bmatrix} i_{C\_3} \\ i_{A\_3} \end{bmatrix} . \tag{10}$$

Based on (8)–(10), the self-inductances L_{CD_23}, L_{AB_23} and the mutual inductance M_{23} in Fig. 13 are solved in

$$\begin{cases} L_{CD\_23} = L_{C\_3} + L_{D\_2} + 2M_{CD\_23} \\ L_{AB\_23} = L_{A\_3} + L_{B\_2} + 2M_{AB\_23} \\ M_{23} = M_{AC\_3} + M_{BC\_23} + M_{AD\_23} + M_{BD\_2} \end{cases} . \tag{11}$$

In Fig. 13, when the two dc-link capacitors are separated, they are on the two parallel current paths from IGBT bridge terminals 2 to 3. Because the dc-link capacitors have impedances, they change the total impedance of each current path. The current flowing through two parallel current paths will be determined by not only the impedances of busbar but also the impedances of dc-link capacitors.

The impedance of a dc-link capacitor is equal to $1/(j\omega C)+j\omega ESL+ESR$. ESR is the equivalent series resistance which is not shown in the figures. If the impedance Z_{C1} and Z_{C2} of the dc-link capacitors is much higher than the impedances of the current paths on the busbar, the current sharing between two current paths is determined by the impedances of dc-link capacitors

$$\begin{cases} \dfrac{i_{C\_3}}{i_{A\_3}} = \dfrac{Z_{C1}}{Z_{C2}} \end{cases} . \tag{12}$$

If the impedances of two dc-link capacitors are equal, two current paths conduct almost identical total currents.

If the impedances of dc-link capacitors are much smaller than those of the busbar, the current sharing between the two current paths on the planar busbar is determined by the current path inductances of the planar busbar even if the dc-link capacitors are separately connected to the busbar. More currents always flow to the path with lower inductance on the planar busbar.

During the transition from states 10 to 11, the self- and mutual inductances in Fig. 15 are derived in

$$\begin{cases} L_{CD\_23} = L_{C\_3} + L_{D\_2} + 2M_{CD\_23} \\ L_{AB\_23} = L_{A\_3} + L_{B\_2} + 2M_{AB\_23} \\ L'_{34} = L_{34} \\ M_{23} = M_{AC\_3} + M_{BC\_23} + M_{AD\_23} + M_{BD\_2} \\ M_{34\_AB} = M_{34\_A} + M_{34\_B} \\ M_{34\_CD} = M_{34\_C} + M_{34\_D}. \end{cases} \tag{13}$$

TABLE I
SIMULATED INDUCTANCE MATRIX

	L_{C_3} (nH)	L_{A_3} (nH)	L_{B_2} (nH)	L_{D_2} (nH)	L_{34} (nH)
L_{C_3}	44.896	2.7708	−17.092	−7.0774	33.646
L_{A_3}	2.7708	12.295	−2.8838	−5.5742	0.81426
L_{B_2}	−17.092	−2.8838	34.684	6.3869	13.902
L_{D_2}	−7.0774	−5.5742	6.3869	31.347	−9.6531
L_{34}	33.646	0.81426	13.902	−9.6531	34.524

TABLE II
CALCULATED INDUCTANCES BASED ON TABLE I

	L_3 (nH)	L_2 (nH)
L_3	10.54	−5.68
L_2	−5.68	18.5

TABLE III
SIMULATED INDUCTANCES

	L_3 (nH)		L_2 (nH)	
L_3	10.42	−1.1%	−4.31	−24%
L_2	−4.31	−24%	19.69	6.4%

TABLE IV
CALCULATED INDUCTANCES BASED ON TABLE I

	L_3 (nH)	L_2 (nH)	L'_{34} (nH)
L_3	10.54	−5.68	6.65
L_2	−5.68	18.5	7.28
L_{34}'	6.65	7.28	−6.30

TABLE V
SIMULATED INDUCTANCES

	L_3 (nH)	L_2 (nH)	L'_{34} (nH)
L_3	10.41	−4.28	6.51
L_2	−4.28	19.73	2.92
L_{34}'	6.51	2.92	12.63

TABLE VI
CALCULATED BASED ON TABLE I

	L_{CD_23} (nH)	L_{AB_2} (nH)
L_{CD_23}	62.09	−13.51
L_{AB_23}	−13.51	41.21

TABLE VII
CALCULATED INDUCTANCES BASED ON TABLE I

	L_{CD_23} (nH)	L_{AB_23} (nH)	L'_{34} (nH)
L_{CD_23}	62.09	−13.51	23.99
L_{AB_23}	−13.51	41.21	14.72
L'_{34}	23.99	14.72	34.52

The current sharing is not derived since during the transition, the current commutates to L_{34} quickly.

The accuracy of the calculated self- and mutual inductances depends on the accuracy of the extracted inductance matrix as equation set (13) is derived rigorously.

IV. SIMULATION VERIFICATION

Simulations were conducted in Maxwell Q3D for switching state 10 and the transition from states 10 to 11. The capacitance of each dc-link capacitor is 3 mF. IGBT bridge switching frequency is 4 kHz. The inductance matrix in (7) was first extracted using Maxwell Q3D. Based on the extracted inductance matrix, the self- and mutual inductances in Figs. 7, 10, 13, and 15 are calculated. Calculation results are compared with the simulated results. The current distributions on both top and bottom plates were also simulated. The relationship of current distributions and inductances are investigated based on the analysis in Section III.

A. Busbar Inductance

In Maxwell Q3D, five current sources were added to IGBT terminal 4, capacitor tabs A, B, C, and D. Two current sinks were added to IGBT terminals 2 and 3. The inductance matrix was extracted in Table I.

The L_2, L_3, and M_{23} for the case with two paralleled dc-link capacitors in Fig. 7 were calculated based on (4) and are shown in Table II. For the case with two paralleled dc-link capacitors, it is possible to use the Maxwell Q3D simulation to directly extract the L_2, L_3, and M_{23} in Fig. 7. The extracted results and the difference from the calculated are shown in Table III.

The calculated self-inductances can match the simulated very well. They have only -1.1% to 6.4% difference. The calculated mutual inductance has -24% difference from the simulated. As Table II is calculated based on the rigorously derived (4), the difference comes from the discrepancy between the simulated inductances in Tables I and III. Either the inaccuracy of the extracted inductances in Table I or the inaccuracy of the inductances in the reduced matrix in Table III could generate the discrepancy. As an example, Maxwell Q3D has limitations on adding sources and sinks; as a result, some inductances in Table I may not be accurately extracted for different switching states or different dc-link capacitor configurations because the proximity effects within different current paths are different.

The self- and mutual inductances during transition from states 10 to 11 in Fig. 10 are calculated based on (7) in Table IV. The directly simulated are in Table V.

Comparing Tables IV and V, L_2, L_3, M_{23}, and M_{3_34} match well, but L'_{34} and M_{2_34} do not match well. Similar to the reason discussed earlier, due to the limitations of the software, either the inaccuracy of the extracted inductances in Table I or the inaccuracy of the inductances in the reduced matrix in Table V could result in the discrepancy.

L_{CD_23}, L_{AB_23}, and M_{23} for the case with two separate dc-link capacitors in Fig. 13 were calculated based on (11) and are shown in Table VI. The self- and mutual inductances during transition from states 10 to 11 in Fig. 15 are calculated based on (13) in Table VII.

For the case with two separated dc-link capacitors, due to the limitations of the software, the self- and mutual inductances cannot be directly extracted. So, the calculated results are not

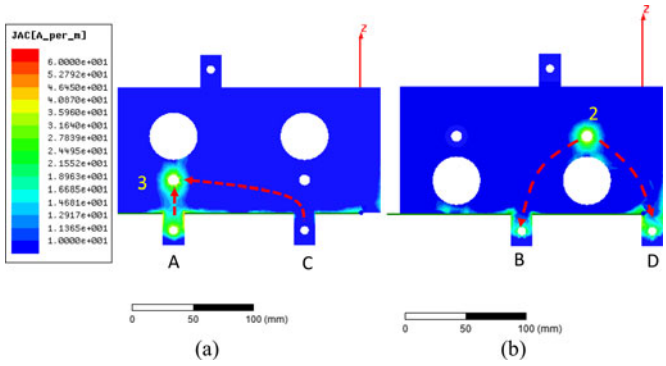

Fig. 16. Current distribution of the busbar when two capacitors are paralleled: (a) top plate and (b) bottom plate.

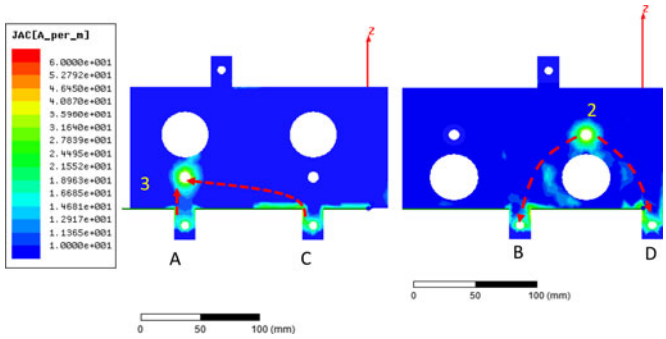

Fig. 17. Current distribution of busbar when two capacitors are separated: (a) top plate and (b) bottom plate.

compared with the simulated results. However, the results will be verified with the measurement results in Section V.

B. Busbar Current Distribution

The busbar's current distributions at switching state 10 for the case when the two dc-link capacitors are paralleled are shown in Fig. 16. Fig 16(a) is for top plate and Fig. 16(b) is for bottom plate.

The current is not evenly distributed because of the impedance difference of currents paths, the proximity effects, and skin effects. For the top plate, because the inductance L_{A_3} is much smaller than L_{C_3}, most of current flows from capacitor tab A to IGBT terminal 3. It has a much higher current density than that from capacitor tab C to IGBT terminal 3. For bottom plate, two current paths have almost the same length and shape, so the current densities have almost the same distribution on the two. This verifies the analysis previously.

Fig. 17 is for the case when the two dc-link capacitors are separated. Because at IGBT bridge's switching frequency 4 kHz, the impedances of the inductances in Table VI are much smaller than that of the 3 mF capacitor dc-link capacitor, capacitor's impedance is dominant. Based on (12), the currents on the two paths are almost equal. Therefore, identical currents were fed to the two current paths in the simulation. Fig. 17(a) is for the top plate and Fig. 17(b) is for the bottom plate.

The current density difference between the current path from capacitor tab C to IGBT terminal 3 and the current path from capacitor tab A to IGBT terminal 3 is much smaller than that in Fig. 16(a). For the same reason as the case in Fig. 16(b), for the bottom plate, the current distributions on two paths are the almost same. This verifies the previous analysis.

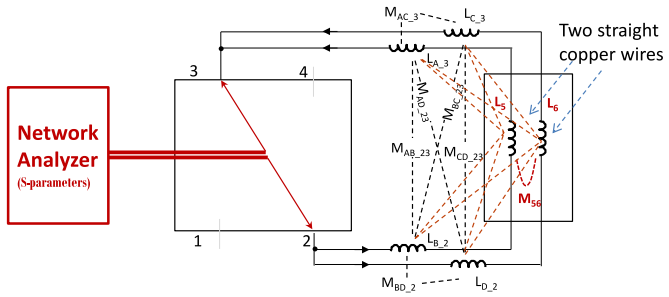

Fig. 18. Measure the loop inductance between IGBT terminals 2 and 3 with all partial inductances and mutual inductances included.

V. Measurement Verification

Because the inductances in Table I are partial self- and mutual inductances of current loops, it is impractical to individually measure these partial self- and mutual inductances in the experiments. It is however practical to measure the loop inductances to verify the simulated and calculated results.

To measure the loop inductances which include all the partial self- and mutual inductances in Table I, capacitor tabs A and B are shorted with a straight copper wire (41.5 mm length and 0.25 diameter). Capacitor tabs C and D are also shorted with a straight copper wire. The inductance L_{23} for the loop starting from IGBT terminals 2 to 3 at switching state 10 and the inductance L_{14} for the loop starting from IGBT terminals 1–4 at switching state 01 were measured. All the self- and mutual inductances of the two copper wires are extracted using Maxwell Q3D. Together with the inductances in Table I, these inductances are used to calculate the loop inductances L_{23} and L_{14}. The measured results will be compared with the calculated results to verify the analysis in this paper.

The loop inductances were measured using one port scattering parameters (*S*-parameters) and then converted to loop inductances based on network theory. S-parameters are easy to more accurately measure than [Z], [Y], and [H] parameters since they do not require ideal open or short [6], [13], [15], [16] in the calibration and measurement. Second, the *S*-parameters can be calibrated to the exact points of the measurement, thus excluding the effects of parasitics [6]. The loop inductance L_{loop} can be derived based on

$$L_{\text{loop}} = \frac{1+S_{11}}{1-S_{11}}\frac{50\Omega}{j\omega}. \tag{14}$$

Fig. 17 shows the measurement setup for the loop inductance between IGBT terminals 2 and 3.

In Fig. 18, after using two copper wires to short the capacitor tabs, L_5, L_6, M_{56}, and other mutual inductances (red dashed lines) are introduced. These introduced inductances were extracted using Maxwell Q3D. The new inductance matrices are shown in Tables VIII and IX.

TABLE VIII
SIMULATED INDUCTANCE MATRIX FOR L_{23}

(nH)	L_{C_3}	L_{A_3}	L_{B_2}	L_{D_2}	L_5	L_6
L_{C_3}	45.00	2.78	−17.07	−6.99	8.64	3.90
L_{A_3}	2.78	12.30	−2.88	−5.57	−1.10	−0.26
L_{B_2}	−17.07	−2.88	34.77	6.38	−2.60	−6.30
L_{D_2}	−6.99	−5.57	6.38	31.42	1.46	3.89
L_5	8.64	−1.10	−2.60	1.46	36.75	1.27
L_6	3.90	−0.26	−6.30	3.89	1.27	36.80

TABLE IX
SIMULATED INDUCTANCE MATRIX FOR L_{14}

(nH)	L_{C_4}	L_{A_4}	L_{B_1}	L_{D_1}	L_5	L_6
L_{C_4}	12.18	2.84	−6.03	−5.52	0.55	−0.85
L_{A_4}	2.84	45.20	6.73	32.98	−9.44	−5.12
L_{B_1}	−6.03	6.73	31.5	27.28	−5.44	−0.91
L_{D_1}	−5.52	32.98	27.28	76.44	−9.60	−11.39
L_5	0.55	−9.44	−5.44	−9.60	36.77	1.33
L_6	−0.85	−5.12	−0.91	−11.39	1.33	36.75

TABLE X
INDUCTANCE COMPARISON

	Calculated based on the model	Measured
L_{23}	39.6 nH	39.8 nH
L_{14}	62.3 nH	65 nH

The loop inductance L_{23} can be calculated from Table VIII based on equation set (15) which was derived in the same way as (11): (15) as shown bottom of the page.

The calculated L_{23} is 39.6 nH. The measured L_{23} in Fig. 19 is 39.8 nH which agrees with the calculated.

Similarly, loop inductance L_{14} can be caculated from Table IX. The caculated L_{14} is 62.3 nH. The measured L_{14} in Fig. 20 is 65.0 nH which agrees with the calculated. Table X shows the comparison between the measured data and the calculated data based on the model.

In Table X, the loop inductance difference is small, which verified the developed technique in this paper.

The inductance circuit model of the busbar when the two dc-link capacitors are paralleled have been verified in Maxwell Q3D simulation in Section IV. Its loop inductance measurement is not conducted here because of the following. First, more pieces of copper wires are needed to parallel and short capacitor tabs to form a inductance loop from the IGBT terminals 2 to 3,

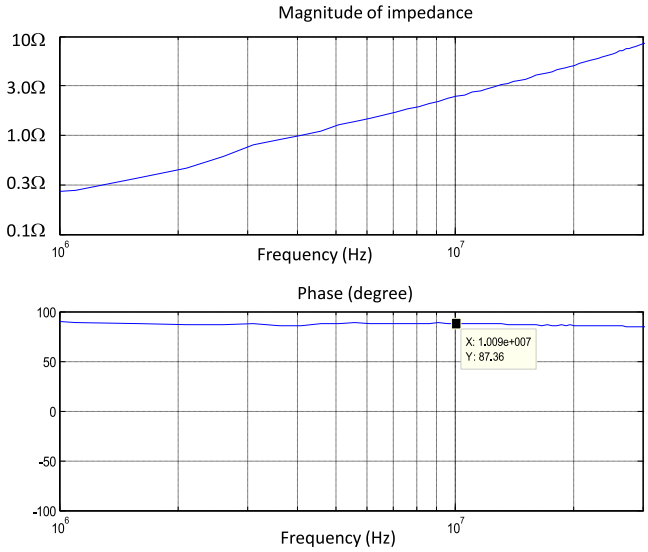

Fig. 19. Magnitude and phase of the measured impedance for loop inductance L_{23}.

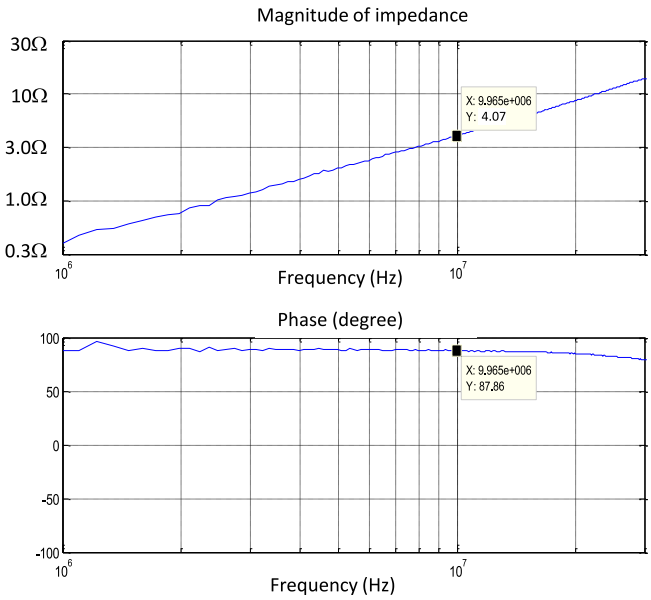

Fig. 20. Magnitude and phase of the measured impedance for loop inductance L_{14}.

$$\begin{cases} L_{23\_CD} = L_{C\_3} + L_{D\_2} + L_6 + 2\left(M_{CD\_23} + M_{6\_C3} + M_{6\_D2}\right) \\ L_{23\_AB} = L_{A\_3} + L_{B\_2} + L_5 + 2\left(M_{AB\_23} + M_{5\_A3} + M_{5\_B2}\right) \\ M_{23} = M_{AC\_3} + M_{BC\_23} + M_{AD\_23} + M_{BD\_2} + M_{56} \\ \quad + M_{6\_A3} + M_{6\_B2} + M_{5\_C3} + M_{5\_D2} \\ L_{23} = \dfrac{L_{23\_CD} L_{23\_AB} - M_{23}^2}{L_{23\_CD} + L_{23\_AB} - 2M_{23}} \end{cases} \tag{15}$$

or from 1 to 4. The self- and mutual inductances of the current paths on the busbar and all the wires need to be extracted. Second, due to the limitations of adding current source and current sink in Maxwell Q3D, it is impossible to extract all the inductances for current paths and copper wires under the condition described earlier. Third, since the inductance matrix cannot be extracted, the loop inductance cannot be caculated. The measured loop inductances thus cannot be used to verify the developed model.

VI. Conclusion and Future Work

This paper first investigates the current paths on a planar busbar as a function of switching states, dc-link capacitor structures, and the connections of dc-link capacitor, IGBT, and filter inductors. Based on the identified current paths, busbar's equivalent inductance circuit models which include both self- and mutual inductances are developed for different switching states, different transition states, and different dc-link capacitor configurations. The technique to reduce the equivalent inductance circuit models is developed and the current sharing of different current paths is explored. Simulations are conducted in Maxwell Q3D and measurements are conducted with *S*-parameters to verify the developed technique.

For future work, the parasitic model of the IGBT bridge module will be explored and developed. With both the busbar inductance model and the parasitic model of the IGBT bridge, a circuit model will be developed for circuit simulations. Time-domain simulations will be conducted to investigate the effects of the inductance of the busbar on inverter's switching behavior. Frequency-domain simulations will be conducted to investigate the effects of the inductance of the busbar on inverter's EMI performance. Experiments will also be conducted to validate the developed circuit model.

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