

# Common Mode Noise Reduction for Boost Converters Using General Balance Technique

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**Abstract**—In this paper, the boost converter model for electromagnetic interference noise analysis is first investigated. Based on this model, a general balance concept is proposed to cancel the common mode noise. Theoretical analysis, simulation, and experiment prove that the proposed balance technique is efficient enough to reduce common mode noise.

**Index Terms**—Balance, common mode (CM) parasitic capacitance, power factor correction, wheatstone bridge.

## I. INTRODUCTION

FRONT-END boost power factor correction (PFC) converters generate significant common mode (CM) noise which is difficult to control. There are several reasons leading to high CM noise in boost PFC. First, the MOSFET switches between 0 V and line voltage, which leads to relatively large amplitude compared with other switches in dc/dc stages. Second, PFC is located in the front end and there are no isolations such as the transformers before the line impedance stabilization networks (LISNs), which allows the noise to be directly measured. Third, because of the large parasitic capacitance between the drain of the MOSFET and the heat-sink, which is sometimes grounded, the noise can go directly through heat-sink to the ground. Fig. 1 shows the boost PFC circuit and the related CM parasitics between the converter and the ground.

In Fig. 1, the effects of the diode bridge preceding the converter are ignored. Since the line frequency is much lower than the switching frequency, the 50/60 Hz ac voltage source is replaced by a dc voltage source in analysis.  $C_a$  is the parasitic capacitance between the drain of the MOSFET and the ground.  $C_b$  is the parasitic capacitance between the cathode, load, and the ground.  $C_c$  is the parasitic capacitance between the traces, load, and the ground. The load can be the dc/dc converters in latter stages. Impedance of two LISNs is  $50\ \Omega$ .

In practical converters, there are parasitics in the converter, such as the junction capacitance  $C_D$  of the diode  $D$ , the output capacitors  $C_{DS}$  of MOSFET, the winding capacitance EPC of inductor  $L_{BT}$ , and the equivalent series inductance ESL of capacitors. All of these parasitics influence the voltage and current waveforms as well as the CM noise. Much work was carried out to investigate and cancel the effects of parasitics on electromagnetic interference (EMI) noise [1]–[7]. Reference [1] inves-

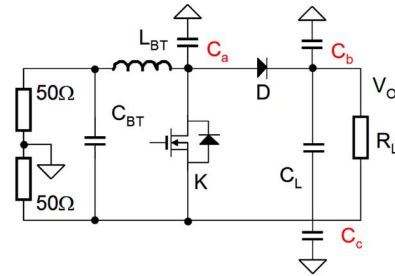


Fig. 1. Boost converter and its CM parasitics.

tigates the effects of parasitics on EMI via simulation and EMI measurement. A method using a cancellation winding coupled to inductors is proposed to reduce the CM noise of converters [2], [3], [6], [7]. Reference [2] first proposed a current balance concept. A perfectly symmetrical circuit was proposed in [5] to generate opposite CM currents with same amplitude to cancel out CM noise.

This paper first investigates the theory of boost converter modeling for EMI. Based on this model, theory and applications employing a general balance concept are proposed to cancel CM noise. Simulation and experiment are carried out to verify the proposed technique.

## II. EMI MODEL FOR BOOST CONVERTERS

The previous work investigates the effects of parasitics by comparing the EMI noise between different parasitic values via simulation and experiment. However, different noise sources are still not identified. The noise path for each noise source is not analyzed. The effects of different noise sources on total CM noise are not decoupled. This section tries to identify different noise sources in boost converters, and then analyze their propagation paths and effects on total CM noise. A systematic theory is developed to describe and predict the CM noise behavior. Based on this theory, the effects of parasitics can be decoupled from total noise, so that the different noise sources can be investigated separately.

The boost converter, including important parasitics is shown in Fig. 2 (not all parasitics are shown in Fig. 2). Due to the parasitics in Fig. 2, there is ringing on switching voltage and current waveforms. Fig. 3 shows the voltage waveform  $V_C$  of MOSFET  $K$ , the current waveform  $I_D$  of diode  $D$ , the voltage waveform  $V_O$  of output capacitor  $C_L$  and the voltage waveform  $V_{C_{BT}}$  of input capacitor  $C_{BT}$ .

According to the substitution theorem, if MOSFET  $K$ , including all the parasitics in the same branch, is substituted by a voltage source  $V_C$  having the same voltage waveform as that

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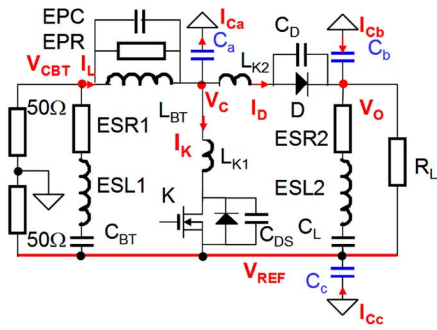


Fig. 2. Boost converter including parasitics.

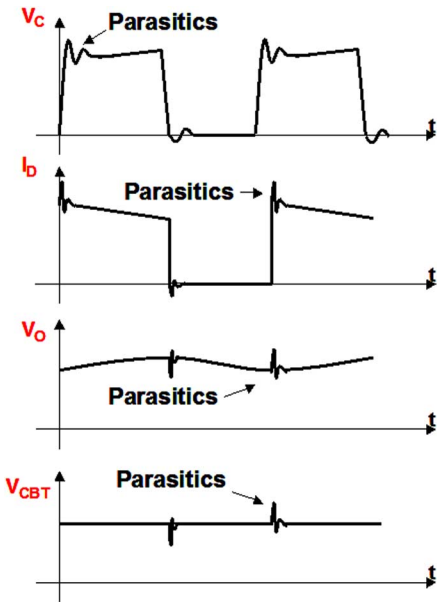


Fig. 3. Voltage and current waveforms.

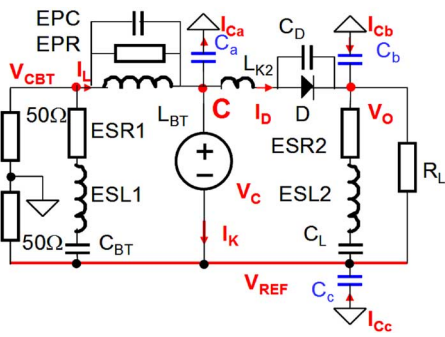


Fig. 4. Substitution of MOSFET with a voltage source.

shown in Fig. 3, the circuit behavior stays the same. Fig. 4 shows the resultant circuit.

After the substitution, based on the theory of Kirchoff's voltage law (KVL), the voltage drop on every branch stays the same. The current on every branch also stays the same because of the constraint of Ohm's law. The diode  $D$ , including all the parasitics in the same branch, can also be replaced by a current source  $I_D$  which has the same waveform as that in Fig. 3. This substitution does not change circuit behavior too.

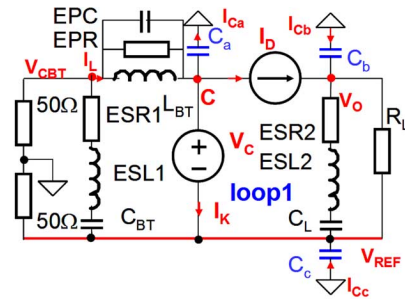


Fig. 5. Substitution of diode with a current source.

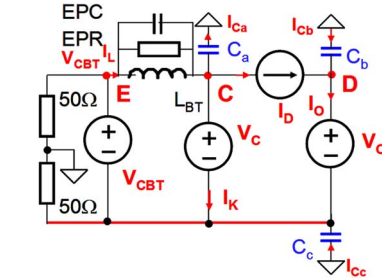


Fig. 6. Boost converter model for EMI analysis.

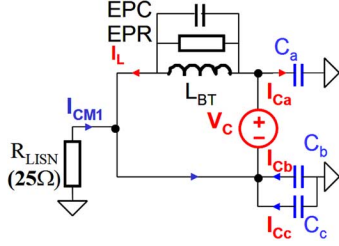
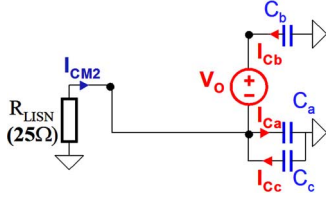
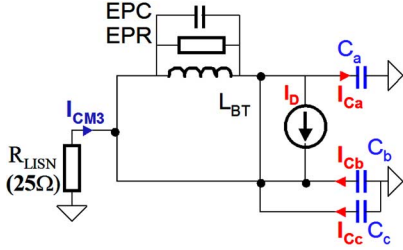
The current on every branch stays the same [Kirchoff's current law (KCL) on node  $C$ ]. The voltage drop on the diode also stays the same because  $V_C$  and  $V_O$  stay the same (KVL on loop1). The resultant network in Fig. 5 is, therefore, equivalent to those in Figs. 2 and 4. It should be pointed out that the internal impedance is zero for voltage source  $V_C$  and infinite for the current source  $I_D$ , which is no longer the time varying impedance as the branch impedances in Fig. 2.

Since the switches are replaced by a voltage source and a current source, the resultant network, with the help of network theory, is much easier, for both CM and differential mode (DM) noise, to analyze than that in Fig. 2.

Because of the parasitics and nonzero impedance of output capacitor, the output voltage  $V_O$  has ripples and spikes as shown in Fig. 3. It is a noise source although its amplitude is much smaller than that of  $V_C$ . Its EMI effects can be best described by the compensation theorem if the impedance of an ideal filtering capacitor is zero. The output capacitor can then be replaced by a noise voltage source, which has the same waveform as that shown in Fig. 3. Following the similar logic, the effects of the voltage  $V_{CBT}$ , which is the voltage on input capacitor  $C_{BT}$ , on EMI noise can also be represented by a noise voltage source which has the same waveform as in Fig. 3. The final model for EMI analysis is then shown in Fig. 6.

Each voltage and current source in Fig. 6 is composed of both dc and ac terms. After the ac and dc terms are decoupled, either of them still meets KCL and KVL. For noise analysis purpose, the ac term is analyzed here. The effects of different noise sources on EMI can be analyzed using the superposition theorem.

The EMI noise on LISNs due to the  $V_C$  (the switching voltage of MOSFET) can be analyzed by replacing other voltage and current sources with their internal impedances. Fig. 7 shows the equivalent circuit.

Fig. 7. Equivalent circuit for finding out the CM noise due to  $V_C$ .Fig. 8. Equivalent circuit for finding out the CM noise due to  $V_O$ .Fig. 9. Equivalent circuit for finding out the CM noise due to  $I_D$ .

In Fig. 7, boost inductor  $L_{BT}$  has no effects on CM noise, since it is in parallel with the noise voltage source. This, however, does not mean  $L_{BT}$  has no effects on total CM noise; its effects are actually included in other voltage sources. CM noise current on LISNs is the difference between current  $I_{Ca}$  and  $I_{Cb} + I_{Cc} \cdot C_b$  and  $C_c$  are parallel with LISNs, so they actually benefit CM noise reduction.  $C_b$  is the only parasitic component leading to CM noise.

Similarly, effects of  $V_O$  can be analyzed in Fig. 8. In Fig. 8, boost inductor does not contribute to CM noise since the voltages on node  $C$  and  $E$  in Fig. 6 are already determined by  $V_C$  and  $V_{CBT}$ .

Effects of current source  $I_D$  are analyzed via Fig. 9. Because the impedances of voltage sources  $V_C$  and  $V_O$  are zero, current source  $I_D$  is shorted. It does not contribute to CM noise. This is reasonable since the voltages on nodes  $C$  and  $D$  in Fig. 6 have been determined by  $V_C$  and  $V_O$ .

For the effects of  $V_{CBT}$ , Fig. 10 shows the equivalent circuit. It is shown that all three parasitic capacitance are in parallel with the LISN at the lower side, so two LISNs are unbalanced. As a result, part of  $V_{CBT}$  is transformed to CM noise as explained by the theory developed in [8].

According to the superposition theory, the total CM noise current flowing through LISNs is the vector sum of four CM currents from Figs. 7–10 as shown in

$$\mathbf{I}_{CM} = \mathbf{I}_{CM1} + \mathbf{I}_{CM2} + \mathbf{I}_{CM3} + \mathbf{I}_{CM4}. \quad (1)$$

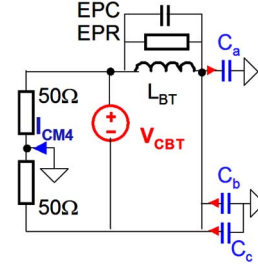
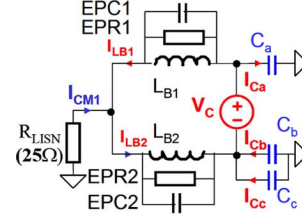
Fig. 10. Equivalent circuit for finding out the CM noise due to  $V_{CBT}$ .

Fig. 11. Splitting the boost inductor.

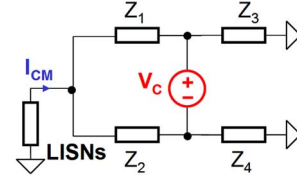


Fig. 12. Wheatstone bridge.

There are two approaches to reduce CM noise. One is to minimize each term and the other one is to cancel each other.

In this section, the EMI noise model is built based on the network theory. Different noise sources are identified. The effects of different noise sources are decoupled so that they can be analyzed separately. Based on these models, the efficient methods for CM noise reduction would, therefore, be possible. For DM noise, the model in Fig. 10 shows that the voltage  $V_{CBT}$  on  $C_{BT}$  is the equivalent noise source.

### III. CM NOISE CANCELLATION WITH BALANCE CONCEPT

Balance concept is proposed in this section to cancel the CM noise generated by different noise sources, which are identified in Section II.

#### A. Reduction of CM Noise Due to $V_C$

In Fig. 7, in order to cancel the CM noise generated by  $V_C$ , i.e., the switching voltage of MOSFET, the inductor is split into  $L_{B1}$  and  $L_{B2}$ . The resultant network is shown in Fig. 11, which looks like a Wheatstone bridge as shown in Fig. 12.

The balance condition for Wheatstone bridge is given as (2). As long as the condition is satisfied, the CM noise current on LISNs is zero

$$\frac{Z_1}{Z_3} = \frac{Z_2}{Z_4}. \quad (2)$$

The corresponding balance condition in Fig. 11 is given by

$$\frac{Z_{LB1}}{Z_{Ca}} = \frac{Z_{LB2}}{Z_{Cb+Cc}} \text{ or } \frac{Z_{LB1}}{Z_{LB2}} = \frac{Z_{Ca}}{Z_{Cb+Cc}} = n. \quad (3)$$

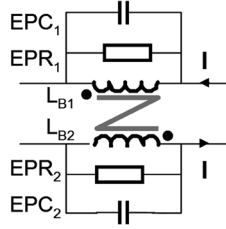


Fig. 13. Two inductors are coupled to balance HF parasitics.

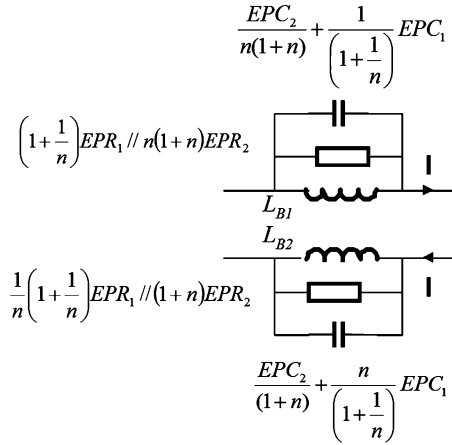


Fig. 14. Decoupled inductors still meet balance condition.

where  $Z_{LB1}$  and  $Z_{LB2}$  are the impedances of two split boost inductors.  $Z_{Ca}$  and  $Z_{Cb+Cc}$  are the impedances of parasitic capacitance. At low frequencies (LF) where the effects of equivalent parallel resistance (EPR) and equivalent parallel capacitance (EPC) are insignificant, the condition (3) is simplified as

$$L_{B1}C_a = L_{B2}(C_b + C_c). \quad (4)$$

Based on the Wheatstone bridge theory, if the boost inductor is split to  $L_{B1}$  and  $L_{B2}$ , and their inductance meets the condition (4), CM noise is canceled. At high frequencies (HF), where inductors are dominated by their parasitics, parasitics must be balanced to cancel CM noise.

Inductors  $L_{B1}$  and  $L_{B2}$  are proposed to be coupled to balance the HF parasitics as shown in Fig. 13.

It is assumed that two inductors in Fig. 13 are perfectly coupled and the noise currents flowing through two inductors are equal (that is the case when the bridge in Fig. 11 is balanced). If the inductance ratio  $L_{B1}/L_{B2}$  that satisfies the balance condition is  $n$ , the decoupled impedances ratio of  $Z_{LB1}/Z_{LB2}$  still meet the condition as shown in Fig. 14. It should be pointed out that  $L_{B1}$  and  $L_{B2}$  here are the decoupled inductance, which is equal to the self inductance plus the mutual inductance. It is easy to prove that if the turn ratio of two inductors is  $n$ , the ratio of two decoupled inductance is also  $n$ , as given by

$$\frac{L_{B1}}{L_{B2}} = n = \text{Turn ratio}. \quad (5)$$

It is also necessary to analyze the effects of the imperfect balance on CM noise. The imperfect balance of Wheatstone

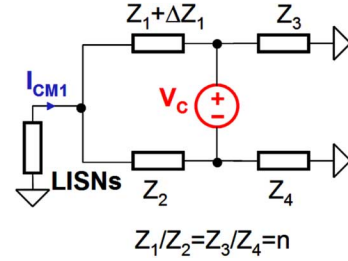


Fig. 15. Effects of unbalance on Wheatstone bridge.

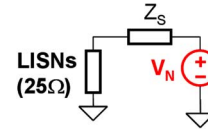
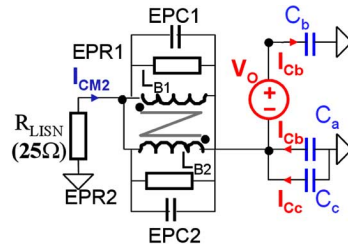


Fig. 16. Thevenin's equivalent circuit.


 Fig. 17. Equivalent circuit for noise source  $V_O$ .

bridge can be described by Fig. 15. Since the balance condition is described by the ratio of two impedances, there would be only one unbalanced component in the Wheatstone bridge. This component can be any one of the four impedances. In Fig. 15, impedance  $Z_1$  is selected as that component. The original four impedances are balanced and the unbalance is introduced by  $\Delta Z_1$ .

Based on Thevenin's theorem, the CM noise model is shown as Fig. 16.  $Z_S$  is the equivalent source impedance, which is given by (6). The  $V_N$ , which is given by (7), is the equivalent CM noise source due to unbalance

$$Z_S = Z_1 // Z_2 + Z_3 // Z_4 \quad (6)$$

$$V_N \approx \frac{\Delta Z_1}{Z_1} \frac{n}{(1+n)^2} V_C. \quad (7)$$

From (7), if the unbalance is characterized by  $\Delta Z_1/Z_1$ , the equivalent CM noise source is proportional to the unbalance. The larger the ratio  $n$ , the smaller the effects of unbalance are. So for the noise generated from  $V_C$ , the effects of unbalance, when  $n$  is large, are not as significant as when ratio  $n$  is small (1 is the smallest ratio).

### B. Reduction of CM Noise Due to $V_O$

After the inductor is split into two coupled inductors as described in Section III-A to balance CM noise caused by  $V_C$ , the equivalent noise model for  $V_O$  is changed from Figs. 8 to 17. It is shown that splitting the inductor cannot reduce the CM noise caused by  $V_O$  because two inversely coupled inductors have zero parallel impedance.



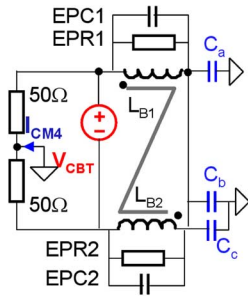


Fig. 18. Equivalent circuit for noise source  $V_{CBT}$ .

There are two possible methods to reduce the CM noise caused by  $V_O$ . The first method is to reduce the ESL and ESR of output capacitors. This actually reduces the noise source  $V_O$ . The second method is to keep  $C_b$  as small as possible. Since  $C_b$  is related to load, it means we have to reduce the parasitic capacitance between the load and the ground.

### C. Reduction of CM Noise Due to $V_{CBT}$

The CM noise model after the inductor is split into two coupled inductors as shown in Fig. 18.

In Fig. 18, two  $50\ \Omega$  LISNs and two inductors form a Wheatstone bridge. Since two LISNs have the same impedance, two inductors should keep a 1:1 impedance ratio to minimize the noise caused by  $V_{CBT}$ . So the turn ratio  $n$  of two coupled inductors should be 1. Using a small equivalent series inductance (ESL) and equivalent series resistance (ESR) capacitor can also reduce the equivalent noise source  $V_{CBT}$ .

### D. Summary

Among three noise sources,  $V_C$  is the major noise because of its largest amplitude. The first step to reduce CM noise should be splitting the boost inductor to balance parasitic capacitance. The second step is keeping the ESL and ESR of the output capacitors as small as possible, which reduces the effects of  $V_O$ . If it is applicable, the inductance ratio of the two inductors should be 1. This may require an extra capacitance parallel with  $C_b$  or  $C_b + C_c$ . The improvement of the different methods on CM noise reduction depends on which noise source is dominant.

## IV. SIMULATIONS AND EXPERIMENTS

The simulations are first carried out in PSpice to verify the theory and the balance idea developed in this paper. A boost converter is then built and the proposed methods are applied. The EMI measurements prove that the proposed balance methods can efficiently reduce CM noise.

### A. Simulation

Simulation is a very easy way to verify the developed theory because all circuit parameters can be easily controlled in the process. The circuit used in PSpice is shown in Fig. 19.  $C_a$  is 40 pF,  $C_b$  is 50 pF, and  $C_c$  is 70 pF. The total inductance of the boost inductors is  $400\ \mu\text{H}$ . The switching frequency is 400 kHz. Fig. 20 shows the simulation results.

Five envelope curves of the simulated CM noise are shown in Fig. 20. The curve1, which has the highest noise, is the CM noise of the original boost converter.

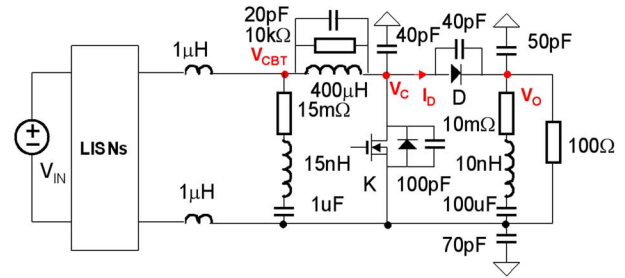


Fig. 19. Simulation circuit for CM noise.

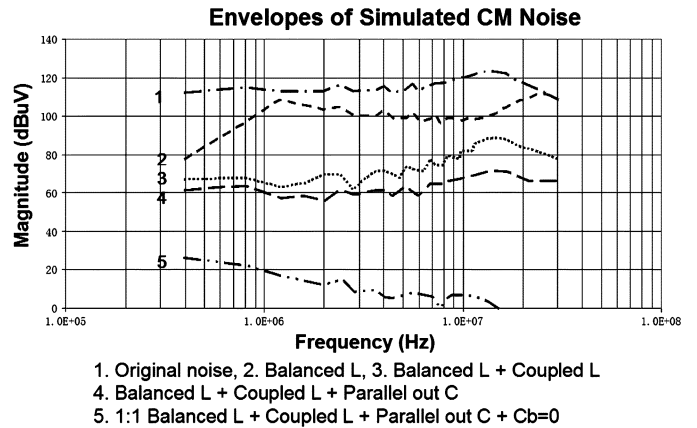


Fig. 20. Simulated envelope curves for CM noise.

The curve2 is the envelope after the boost inductor is split into a  $300\ \mu\text{H}$  and a  $100\ \mu\text{H}$  inductors to balance  $C_a$  (40 pF) and  $C_b + C_c = 120\ \text{pF}$  parasitic capacitance. The improvement at LF is significant; however, because the parasitics of two inductors are no longer balanced at HF, the improvement at HF is limited.

The boost inductor is then split into two coupled inductors. The self-inductance of two inductors is 225 and  $25\ \mu\text{H}$ , respectively. The mutual inductance is  $75\ \mu\text{H}$  if they are ideally coupled. Because decoupled inductance is the sum of self-inductance and mutual inductance, the decoupled inductance of these two inductors is 300 and  $100\ \mu\text{H}$ , respectively. The CM noise is greatly reduced because the HF parasitics are also balanced. Curve3 shows these results. There is a 30–45 dB improvement in whole frequency range compared with curve1. A  $1\ \mu\text{F}$ , small ESL (2 nH) capacitor is then parallel with the output capacitor. Curve4 shows the effects of this small capacitor on CM noise reduction. There is another 5–15 dB improvement since the amplitude of  $V_O$  is reduced. For, curve5 the inductance ratio of two coupled inductor is 1 (two  $100\ \mu\text{H}$  inductors coupled) and one 80 pF capacitor is paralleled with  $C_a$ .  $C_b$  is also set to zero. Because the effects of all three noise sources are minimized, curve5 got the best result. Curve5 is used to verify the theory developed in Section III only. In practical cases, it is impossible to make  $C_b$  zero.

### B. Experiment

A boost converter is built to test the proposed methods. The experiments concentrate on the balance of  $V_C$  because  $V_C$  is the major noise source. This boost converter has the similar schematic as shown in Fig. 19. The switching frequency is 200 kHz. The critical parasitics are first measured.  $C_a$  is 16 pF,

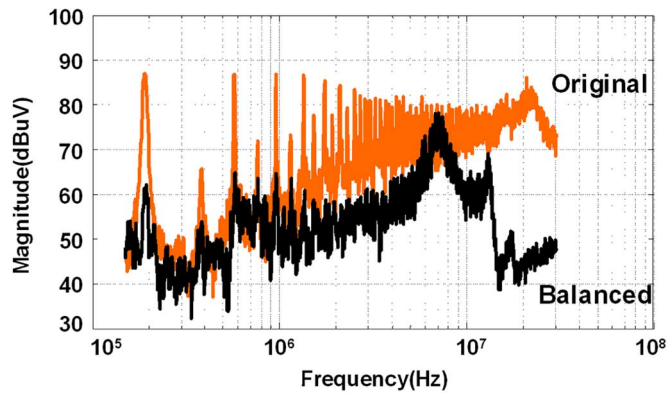


Fig. 21. Comparison of measured CM noise.

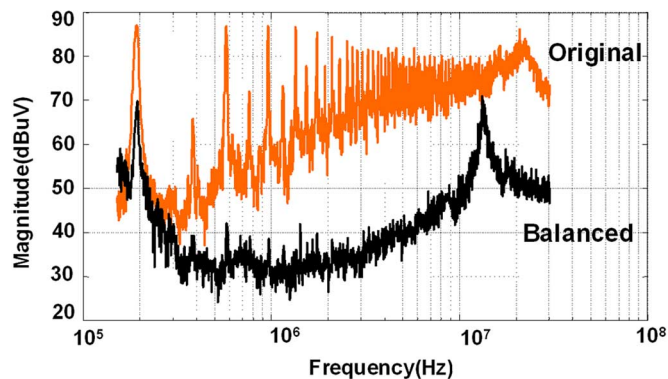


Fig. 22. Comparison of measured CM noise.

$C_b$  is 14 pF, and  $C_c$  is 31 pF. The inductor is then split into two coupled inductors with a 1:1 turn (inductance) ratio. According to the theory in Section III, a 29-pF capacitance should be paralleled with  $C_a$  to balance the CM noise. The measured CM noise before and after paralleling 29-pF capacitance is shown in Fig. 21. There is a 25-dB improvement at 200 kHz and a 20-dB improvement at 30 MHz.

For the second measurement, the coupled inductors have an inductance ratio of 2:1. An 8-pF capacitor is then paralleled with  $C_a$  to balance the bridge, which is a little bit different from the calculated 7 pF. The measured CM noise before and after the balance is shown in Fig. 22. It shows that a 10–50 dB improvement is achieved within the whole frequency range.

In a practical design, it may not be practical to directly measure  $C_b$  and  $C_c$  since they are loads related and the loads are usually dc/dc converters. In those cases, the  $C_b$  and  $C_c$  may be derived from the CM noise measurements. The possible method is to adjust the inductance ratio of the two boost inductors until you get the lowest CM noise when the balance condition is achieved. Since the inductance ratio of two boost inductors is known; and  $C_a$  is known by measurement,  $C_b + C_c$  can be calculated via (4). Another alternative is to fix the ratio of the two boost inductors and then parallel more capacitance with  $C_a$  or  $C_c$  until you get the lowest noise when the balance condition is achieved.  $C_b + C_c$  can then be calculated via balance condition.

Greatly reduced CM noise benefits EMI filter design because of its low attenuation requirement. The EMI filter size with CM noise balance can be much smaller than that without CM noise balance.

In this section, both simulations and CM noise measurements prove that the proposed balance methods can efficiently reduce the CM noise of boost converters. The balance condition can be achieved by adjusting the inductance ratio of two split boost inductors, paralleling small capacitors with parasitic capacitance or doing both.

## V. CONCLUSION

In this paper, the EMI noise model for boost converters is first built based on the network theory. Different noise sources are identified and their effects on CM noise are decoupled. The effects of different noise sources on CM noise can therefore be investigated separately. A general balance concept is then introduced to cancel the CM noise of boost converters. The methods to improve balance are also discussed. Finally, the simulations and experiments prove that the proposed methods can efficiently reduce CM noise.

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