Common Mode EMI Noise Suppression for Bridgeless PFC Converters

Pengju Kong, Shuo Wang, *Senior Member, IEEE*, and Fred C. Lee, *Fellow, IEEE*

***Abstract*—The goal of this paper is to study the possibility of minimizing common mode (CM) noise emission in bridgeless power factor correction (PFC) converters. Two approaches are proposed. In the first approach, the bridgeless PFC is modified to achieve symmetry. A CM noise model for symmetric topology is derived and the conditions for symmetry are summarized. Parasitics critical to the symmetrical condition are studied and carefully controlled. As a result, CM noise can be minimized with good cancellation. The second approach is to introduce a balance technique to bridgeless PFC converters. The topology is modified so that the balance technique can be applied so as to minimize CM noise. Experimental results validate that both approaches can greatly reduce CM noise up to 30 dBμV. The two approaches are compared in terms of both its effects on CM noise and their implementations.**

***Index Terms*—Balance, bridgeless power factor correction (PFC) converter, common mode (CM) noise, symmetry.**

I. Introduction

In recent years, significant efforts have been made to achieve higher efficiency on active power factor correction (PFC) converters. The bridgeless PFC is one of the most attractive PFC topologies, which achieves high efficiency by eliminating the line-voltage bridge rectifier [1]. Compared to the conventional boost PFC implementations, it eliminates the line-voltage bridge rectifier so that the conduction loss is reduced [2]. However, this topology emits much higher conducted common mode (CM) electromagnetic interference (EMI) noise than conventional boost PFC converters. Significantly larger CM chokes are needed in order to meet the EMC standards. As a result the cost is increased and the power density is reduced.

Some analysis and modeling work on the CM noise of the bridgeless PFC has been done and reported in [3] and [4]. It is indicated that, in a bridgeless PFC converter, the voltage potential of the output bus in regard to ground is pulsating. Large parasitic capacitance between the output bus and ground provides a relatively low impedance path so that CM noise is high. Modifications on the bridgeless PFC topology were proposed in [4] and [5]. By stabilizing the voltage potential of the output bus, both solutions reduce the CM noise level of the converter to the same as that in a conventional boost PFC. However, the boost inductance is twice of a boost PFC converter.

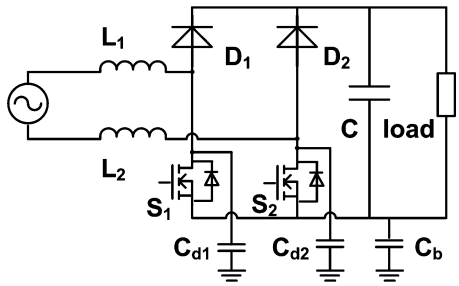

Fig. 1. Topology of bridgeless PFC with parasitic capacitances to ground.

It is possible to further reduce the CM noise of the bridgeless converter with CM noise cancellation techniques. CM noise cancellation techniques using a balance concept have been proposed and implemented in power converters in [6]–[12]. In papers [6]–[8], a cancellation winding coupled with boost inductor or transformer is used to generate CM noise-canceling current. In paper [9] and [10], a balance concept is proposed to reduce CM noise. A modification of the converter was made to achieve topological symmetry. In a symmetric topology, CM noise currents are always out of phase so that they cancel each other. In [11] and [12], the balance concept is extended and generalized. Symmetry is no longer necessary. These techniques can be applied to a bridgeless converter to further reduce CM noise.

In this paper, two approaches to minimize CM noise in bridgeless PFC converters are proposed and compared. One approach is to modify the topology to achieve total symmetry. The CM noise model is derived to model the symmetric topology, and important parasitics that affect topological symmetry are studied. By achieving symmetry in topology, CM noise can be minimized. The other approach is to implement the balance technique proposed in [11] in the bridgeless PFC. In order to apply the balance technique, a modification in topology is needed to reduce CM noise for the whole line cycle. Experiments are done to validate the two approaches, and it is shown that both can effectively reduce CM noise to a very low level. Design considerations for both approaches are discussed.

II. Bridgeless PFC and Its CM Noise

The topology of a bridgeless PFC with parasitic capacitance to ground is shown in Fig. 1. It has two working sub-periods which correspond to the polarity of the input voltage. In the positive half-line cycle, L_1, L_2, D_1 and S_1 serve as a boost

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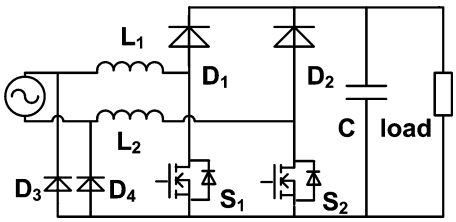

Fig. 2. Topology of bridgeless PFC proposed in [5].

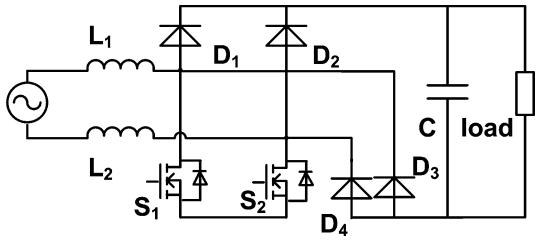

Fig. 3. Symmetric topology of bridgeless PFC converter.

converter, while the body diode of S_1 provides a current return path. In the negative half-line cycle, L_1, L_2, D_2 and S_2 serve as a boost converter, while the body diode of S_1 provides a current return path. There is an alternative topology of the bridgeless PFC with only one inductor. In that case L_2 is zero.

As we all know, CM noise is due to the voltage pulsating generated by high-frequency switching. Such high dv/dt generates CM noise currents which go through the parasitic capacitance from converter to ground. In order to address the CM noise issue, parasitic capacitances to ground are also shown in Fig. 1. C_{d1} and C_{d2} are drain-to-ground capacitance of S_1 and S_2. C_b is the parasitic capacitance between the ground and the output bus, which includes the control circuit, output bus traces and the load. The measured C_{d1} and C_{d2} are ranging from 10 to 40 pF. And the measured C_b is between 200 and 500 pF.

In a conventional boost PFC, which is a diode bridge followed by a boost converter, the output bus is always connected to the input power line through the conducting input diode bridge. The only parasitic capacitance contributing to CM noise is the drain-to-ground capacitance. In a bridgeless PFC, because of the two inductors on the input, the voltage potential of the output bus is pulsating with the amplitude of half of the output voltage. C_b provides a relatively low impedance path for CM current so that high CM noise is observed. Solutions which reduce the CM noise of bridgeless PFC converters to the same level as boost PFC were proposed in [4] and [5]. Fig. 2 shows the topology proposed in [5]. Two diodes are added in the bridgeless PFC topology to provide a path between the input and output bus, so that the voltage potential of output bus is stabilized.

III. CM Noise Suppression via Symmetric Topology Approach

A. Symmetric Topology of Bridgeless PFC

The symmetric topology concept was proposed in [9] and demonstrated in a boost PFC. A symmetric topology generates out-of-phase noise currents with the same amplitude. Therefore, these currents cancel each other and CM noise is confined in the converter. There is no CM noise measured in LISNs. However, one diode is added to the topology and conduction loss is increased.

Achieving symmetry in a bridgeless PFC can reduce CM noise while the conduction loss stays the same. This makes the concept more attractive. As shown in Fig. 3, two diodes are inserted to the return path of the output bus, which makes the topology symmetric. Since the current goes through these diodes instead of through the body diode of MOSFET, the conduction loss of this topology is the same as the original bridgeless PFC.

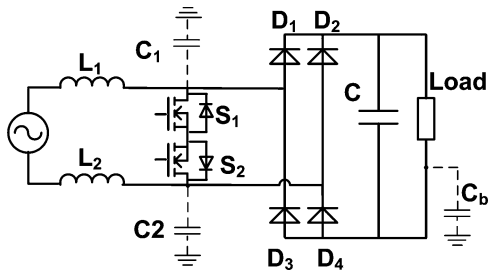

Fig. 4. Symmetric topology of bridgeless PFC converter (re-organized).

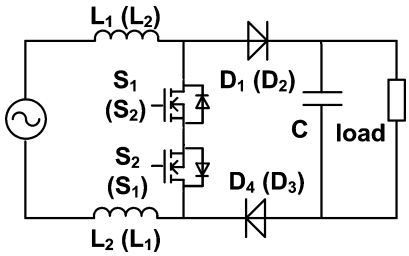

Fig. 5. Simplified topology for symmetric bridgeless PFC in half-line cycles.

For a better understanding, this symmetric topology is redrawn in Fig. 4 and all parasitic capacitances are included. This topology consists of a bidirectional switch followed by a diode bridge. The bidirectional switch is implemented with two MOSFETs in series. C_1 consists of the drain-to-ground capacitance of S_1 and cathode-to-ground capacitance of D_3, while C_2 consists of parasitics introduced by S_2 and D_4.

In a positive half-line cycle, the current flows through S_1 and the body diode of S_2. D_1 and D_4 also conduct current in this half-line cycle. So the topology in the positive line cycle can be simplified, as shown in Fig. 5. Current direction in the negative half-line cycle is the opposite of the positive half-line cycle, so that S_2, the body diode of S_1, D_2 and D_3 conduct. Its simplified topology is exactly the same as that in a positive half-line cycle except that components are changed. The component names for a negative half-line cycle are shown in brackets in Fig. 5.

After this simplification, the topologies in both half-line cycles are exactly the same as the topology proposed in [9], which is proven to have low CM noise. However, understanding of this topology is still limited. A CM noise model is needed to study the effects of this topology and its parasitics on CM noise.

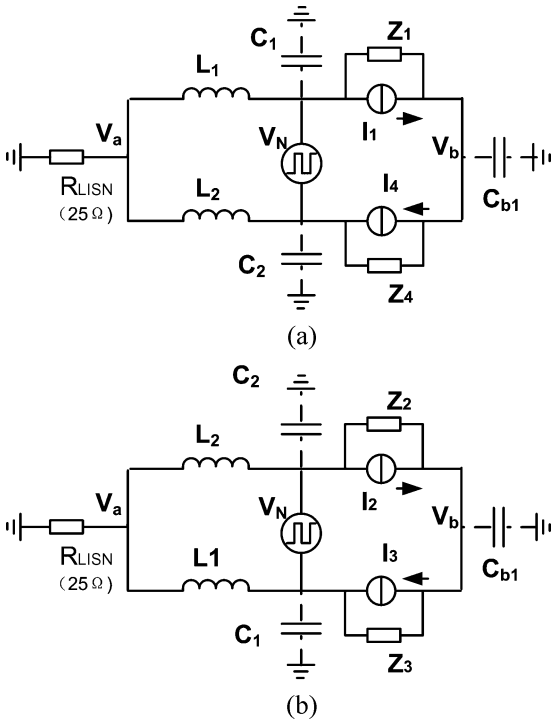

Fig. 6. CM noise model for symmetric bridgeless PFC in half-line cycles: (a) positive half-line cycle and (b) negative half-line cycle.

B. CM Noise Model of Symmetric Bridgeless PFC

In the conventional boost PFC modeling methods used in [3] and [11], the MOSFET branch is modeled as a voltage source. The output capacitor is treated as a short circuit since its impedance in the EMI frequency range is very small. The switching diode is then in parallel with a voltage source. It is modeled by a current source and its effects are absorbed in the voltage source. So there is only one noise source in the noise model. On the input side, there is usually an input capacitor which can be modeled as short circuit. The LISNs are modeled as two 50 Ω resistors in parallel [13].

However, in the symmetric bridgeless PFC there are two more diodes in the topology; thus modeling becomes complicated. Take the positive half-line cycle as an example for CM noise modeling. The body diode of S_2 can be treated as short circuit. For the diodes D_1 and D_4, since parasitics have a great impact on the voltages across the diodes, a simple current source model does not provide enough information. A more deliberate model for diodes should be used. Here a current source in parallel with one source impedance is used to represent the characteristic of a diode and all parasitics on its branch. Such a modeling approach was used in [14]. As a result, in the noise model of a symmetric PFC, there are three sources, as shown in Fig. 6. One voltage source represents the MOSFET branch. Two current sources with source impedances represent the two diodes' branches. Ideally, for the same type of diodes with the same characteristics and the same parasitics, the two current sources are identical.

The CM noise model for a negative half-line cycle again has the same topology as the positive cycle.

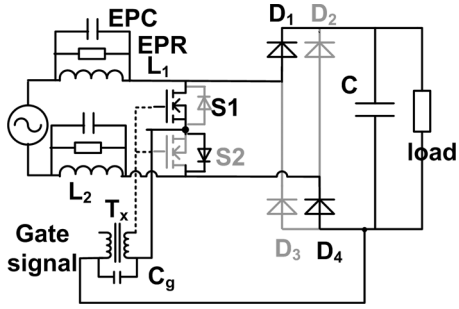

Fig. 7. Positive half-line cycle with parasitic effects.

C. Conditions of Symmetry to Minimize CM Noise

The model shown in Fig. 6 is symmetric in topology. To minimize the CM noise, all the parameters in the structure should be symmetric. The conditions for minimizing CM noise are:

A) $C_1 = C_2$;
B) $I_1 = I_4$ (positive half-line cycle), and $I_2 = I_3$ (negative half-line cycle);
C) $Z_1 = Z_4$ (positive half-line cycle), and $Z_2 = Z_3$ (negative half-line cycle);
D) $Z_{L1} = Z_{L2}$.

Under these conditions, V_a and V_b in Fig. 6 will both be equal to half of the voltage of noise source V_N. The CM current does not flow through LISN or C_b.

For condition A, the nature of C_1 and C_2 has already been discussed. By fixing S_1 and S_2 on the same heatsink and D_3 and D_4 on the same heatsink, it is easy to achieve this condition.

For condition B, I_1 and I_4 (I_2 and I_3 in negative half-line cycle) represent the current on two diodes in series; ideally these two sources are the same if two diodes are exactly the same.

For condition C, the positive half-line cycle is analyzed as an example. An important part of Z_1 and Z_4 is the junction capacitances of diodes, with a typical value of 50 pF. For the same type of diodes, junction capacitances are equal to each other. However, condition C cannot be met in both half-line cycles due to the parasitic effects of the gate drive transformer, as shown in Fig. 7. C_g is the parasitic capacitance between the primary side and the secondary side of the gate drive transformer and it is equivalently in parallel with D_4. So C_g is part of Z_4 and introduces asymmetry into the topology. The typical value of C_g is around 50 pF, which is the same in range as the value of the junction capacitances, so its effects are significant. As a result, such a 'symmetric topology' is not perfectly symmetric. CM noise emission of the symmetric topology is much lower than the original bridgeless PFC but only a little lower than the topologies proposed in [4] and [5].

For condition D, the impedance of L_1 and L_2 should be equal. Fig. 7 includes a high-frequency model of inductor L_1 and L_2. The impedance of an inductor is determined by its inductance in the low-frequency range, which can be control in the inductor design procedure. However, in the high-frequency range, its impedance is determined by its equivalent parallel capacitance (EPC) and equivalent parallel resistor (EPR), which are parasitics and not easy to control.

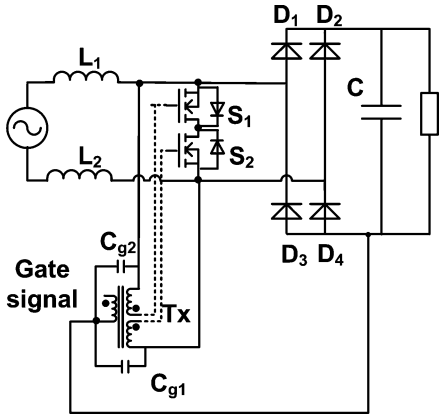

Fig. 8. Improved symmetric bridgeless PFC with gate drive transformer.

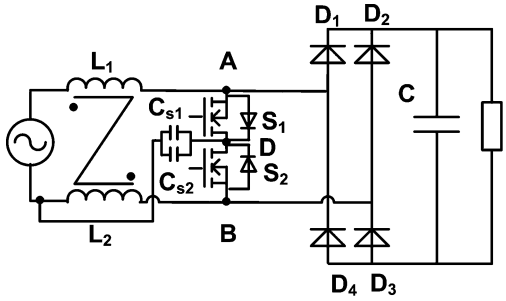

Fig. 9. Improved symmetric bridgeless PFC with heat-sink connected to power line.

D. Improved Symmetric Topology With Minimized CM Noise

In the symmetric topology, as shown in Fig. 4, two MOSFETs are in series with their sources connected to each other. To solve the issue caused by C_g, the topology is changed, as shown in Fig. 8, where two MOSFETs are in series with their drains connected. A two-second-winding transformer is used to provide isolated gate drives. C_{g1} and C_{g2} are introduced symmetrically. They are part of the source impedance of the current sources for the diodes. In the positive half-line cycle in Fig. 6, C_{g1} is part of Z_1 and C_{g2} is part of Z_4 and they are symmetric. The same conclusion can be made for the negative half-line cycle.

However, the topology modification also changes the parasitic capacitances to ground, as shown in Fig. 9. C_{s1} and C_{s2}, the drain to ground capacitances of S_1 and S_2, move from nodes A and B to D. To achieve symmetry, their effect should be minimized. The heat-sink for S_1 and S_2 is directly or via a capacitor connected to the power line so that drain-to-ground capacitances become drain-to-line capacitances. In the positive half-line cycle, C_{s1} and C_{s2} are in parallel with L_2, while in the negative half-line cycle they are in parallel with L_1. They become part of the EPC of the inductors.

To satisfy condition D, the impedances of L_1 and L_2 should be the same under all working conditions in the whole EMI frequency range. At the high frequency range, the impedance of the inductor is determined by its EPC and EPR, which are not easy to control. Coupling L_1 and L_2 into one core can solve this issue [11]. By coupling L_1 and L_2, the impedance ratio of L_1 and L_2 is only determined by the turns ratio if the coupling coefficient is 1. In this topology, a 1:1 turns ratio is adopted to satisfy condition D so that $Z_{L1} = Z_{L2}$. However, in practice, coupling coefficient k can not be unity. As a result, the ratio of Z_{L1} and Z_{L2} becomes:

$$\frac{Z_{L1}}{Z_{L2}} = \frac{L + j2\pi f L^2(1-k)/Z_{e2}}{L + j2\pi f L^2(1-k)/Z_{e1}}. \tag{1}$$

L is the self inductance of L_1 and L_2. k is the coupling coefficient between L_1 and L_2. Z_{e2} is the impedance of EPC and EPR of L_2, and Z_{e1} is the impedance of EPC and EPR of L_1. Since impedance of EPC is dominant in Z_{e1} and Z_{e2}. (1) is simplified as

$$\frac{Z_{L1}}{Z_{L2}} = \frac{L - 4\pi^2 f^2 L^2 EPC_2(1-k)}{L - 4\pi^2 f^2 L^2 EPC_1(1-k)}. \tag{2}$$

At low frequency range, L is dominant in both the numerator and the denominator, as is expressed in math in (3). n is introduced as the acceptable tolerance to denote the fact that how dominant L should be. The value of n is specified as 20% in this paper. As long as (3) is satisfied, (2) is equal to 1 and independent on frequency. Condition D is satisfied. When frequency increases, parasitic effects become dominant. Z_{L1} is no longer equal to Z_{L2}. Condition D is not valid and CM noise will be higher. In other word, symmetry can be only achieved in the low frequency range. The upper frequency of this range is defined in (4), which is derived from (3)

$$\begin{cases} nL \geq 4\pi^2 f^2 L^2 EPC_2(1-k) \\ nL \geq 4\pi^2 f^2 L^2 EPC_1(1-k) \end{cases} \tag{3}$$

$$f_k = \min\left(\sqrt{\frac{n}{4\pi^2 L * EPC_1(1-k)}}, \sqrt{\frac{n}{4\pi^2 L * EPC_2(1-k)}}\right). \tag{4}$$

From (4), it can be seen that higher coupling coefficient k can achieve higher upper frequency. In the prototype built for experiments, $L = 50$ μH and EPC= 40 pF. In order to achieve symmetry up to 30 MHz, which is the upper frequency of conducted EMI frequency range, k should be as high as 0.997.

In general practice, two windings are wound separately on two halves of the core, as shown on the left of Fig. 10. With such winding technique coupling coefficient is relatively low, 0.77 in this prototype. The bifilar winding technique is adopted to achieve a high coupling coefficient [15]. As shown on the right of Fig. 10, with bifilar windings, k is 0.997. Symmetry can be achieved in the entire conducted EMI frequency range.

The two coupled inductors shown in Fig. 10 were put in the improved symmetric bridgeless PFC prototype and CM

Fig. 10. Coupled boost inductors with different winding techniques (1:1 turn ratio).

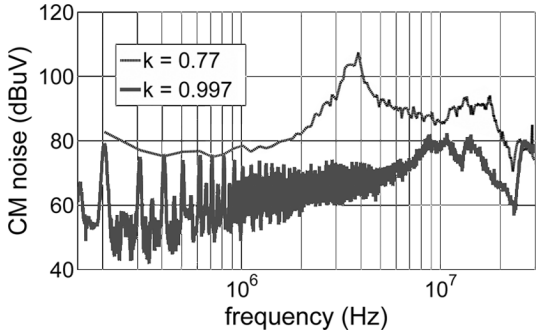

Fig. 11. Effects of coupling coefficient on CM noise.

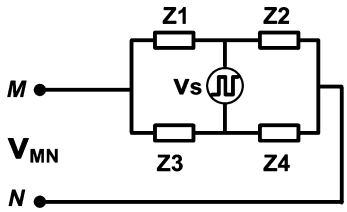

Fig. 12. Wheatstone bridge.

noises are measured. The measurement setups are specified in Section IV. Fig. 11 shows the effects of the coupling coefficient of the boost inductors on CM noise. With separate windings, k is 0.77. Symmetry can not be satisfied at high frequency. CM noise becomes high after 2 MHz. With bifilar windings, k is 0.997. The CM noise stays low in the whole frequency range.

With all these modifications, an improved symmetric topology for a bridgeless PFC is developed, as shown in Fig. 9. This topology can further reduce CM noise compared to the original symmetric topology mentioned in Section III-A.

IV. CM Noise Suppression via Balance Approach

The symmetry solution achieves minimum CM noise with the cost of two additional diodes and a gate drive transformer. The balance technique proposed in [11] provides an opportunity to reduce CM noise with less cost.

A. Balance Concept and Its Effect on CM Noise

A balance concept was proposed in [11]. A general form of the Wheatstone bridge is shown in Fig. 12. As long as the impedances on the four bridge legs satisfy the balance condition

$$\frac{Z_1}{Z_3} = \frac{Z_2}{Z_4} \tag{5}$$

the voltage between node M and N is always zero, regardless of the characteristic of voltage source V_s.

In the derived CM noise model of a bridgeless PFC in Fig. 13, the bridge is composed of V_N, the boost inductances and parasitic capacitances. This provides an opportunity to utilize the Wheatstone bridge to balance the bridge so as to minimize CM noise.

B. Balancing the Bridgeless PFC to Minimize the CM Noise

The CM noise model for a bridgeless PFC was derived in [3]. Models for both half-line cycles are shown in Fig. 13.

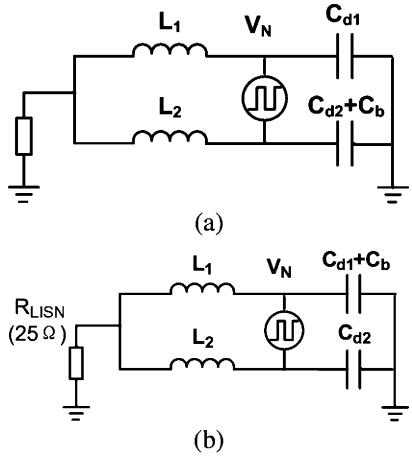

Fig. 13. CM noise models of bridgeless boost PFC for two half-line cycles: (a) positive half-line cycle and (b) negative half-line cycle.

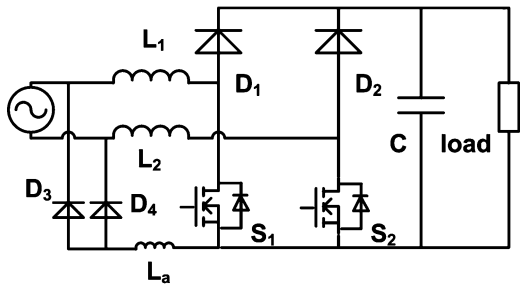

Fig. 14. Bridgeless PFC using balance technique.

To implement the balance technique in the bridgeless PFC to minimize CM noise, the balance condition should be satisfied in both half-line cycles. For the positive half-line cycle, (6) should be satisfied, while for the negative half-line cycle, (7) should be satisfied

$$\frac{Z_{L1}}{Z_{L2}} = \frac{Z_{Cd1}}{Z_{Cd2+Cb}} \tag{6}$$

$$\frac{Z_{L1}}{Z_{L2}} = \frac{Z_{Cd1+Cb}}{Z_{Cd2}}. \tag{7}$$

Obviously (6) and (7) cannot be satisfied simultaneously, so balance cannot be achieved by simply adjusting the ratio of L_1 and L_2.

A small inductor and two diodes are introduced to help balancing both half-line cycles, as shown in Fig. 14. In the positive half-line cycle, L_a is in parallel with L_2, while in the negative half-line cycle L_a is in parallel with L_1. As a result the CM noise models and balance conditions are changed, as shown in

$$\frac{L1}{L2//La} = \frac{Cd2+Cb}{Cd1} \tag{8}$$

$$\frac{L2}{L1//La} = \frac{Cd1+Cb}{Cd2}. \tag{9}$$

There are numerous solutions to satisfy both (8) and (9). To make the design simple, let $C_{d1} = C_{d2}$ and $L_1 = L_2$, so that (8) and (9) merge into (10). Here, $C_d = C_{d1} = C_{d2}$ and $L =$

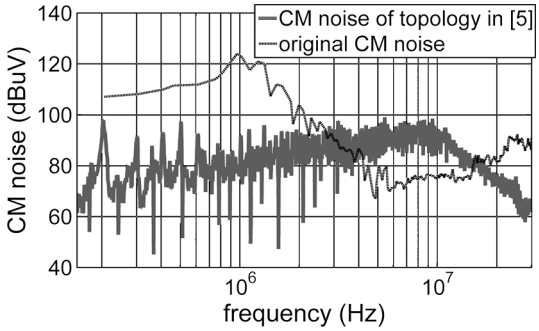

Fig. 15. CM noise comparison between the original bridgeless PFC and the topology proposed in [5].

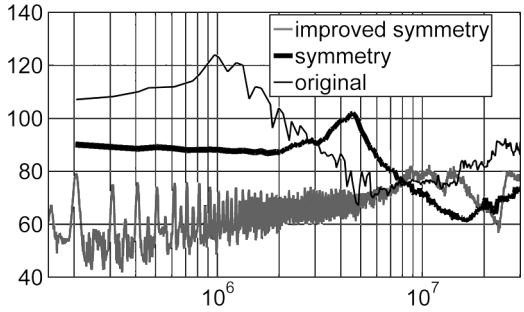

Fig. 16. CM noise comparison between original, symmetric and improved symmetric bridgeless PFC.

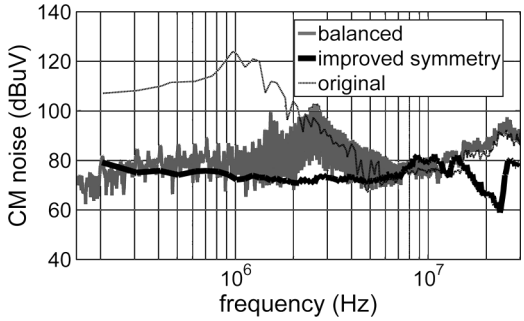

Fig. 17. CM noise comparison between original, improved symmetric and balanced bridgeless PFC.

$L_1 = L_2$. Once (10) is achieved in the converter, CM noise can be minimized.

$$\frac{La}{L} = \frac{Cd}{Cb}. \tag{10}$$

One issue in the balance approach is that the inductors can not be coupled for this case so that the high-frequency noise is not as low as it is in the symmetric approach.

V. Experiment Verification

A. Experiment Setup

Five 500 W bridgeless boost PFC converters are built to validate the proposed methods. All of them have 110 V ac input, 400 V dc output and 100 kHz switching frequency.

The first converter is the original bridgeless boost PFC, as shown in Fig. 1. L_1 and L_2 are both 100 μH. Parasitic capacitances of the converter were measured: C_{d1} and C_{d2} are 31 pF and C_b is 425 pF. The second converter uses the topology in Fig. 2. The inductance of L_1 and L_2 is two times of the original to keep the same input current ripple. The third converter is the balanced bridgeless PFC, as shown in Fig. 14. To balance the bridgeless PFC, a L_a of 14.6 μH is added. The fourth converter built is symmetric bridgeless PFC in Fig. 4. L_1 and L_2 are coupled and the total boost inductance is 200 μH. The fifth converter is the improved symmetric bridgeless PFC in Fig. 8. It has almost the same layout as the fourth converter.

B. CM Noise Measurement

In experiments, every CM noise result in this paper is measured under the condition that the converter prototype runs in an EMI chamber at full load with 110 V ac input. LISNs are connected to the input of the prototype and an Agilent EMC 7402 EMC analyzer is used for EMI measurement. A noise separator proposed in [16] is used to extract CM noise from the total noise. All CM noises are measured with peak mode.

Fig. 15 shows the CM noise comparison between the original bridgeless boost converter and the topology in Fig. 2. The dotted line is the envelope of CM noise of the original bridgeless PFC converter. The CM noise in the low-frequency range is greatly reduced.

Fig. 16 shows the CM noise envelope of the original bridgeless FPC, the symmetric topology and the CM noise spectrum of improved symmetric topology. By achieving symmetry, CM noise can be reduced by 30 dBμV at 200 kHz.

Fig. 17 shows the CM noise of the balanced bridgeless PFC. By balancing the converter, CM noise can be reduced. The noise peak at 200 kHz is reduced by 27 dBμV compared to the original design, and 15 dBμV compared to the topology in Fig. 2. However, noise between 1 and 4 MHz is still high due to the high frequency parasitics.

VI. Conclusion

Two approaches for minimizing CM noise emission in a bridgeless PFC have been proposed in this paper. One approach takes efforts to achieve symmetric topology. For this approach, the total inductance stays the same, while two more diodes and a gate drive transformer are needed. The second approach is to apply the balance concept. A small inductor is added to achieve balance; hence the CM noise is reduced. Important parasitic capacitances affecting the balance or symmetry conditions are also studied in detail. Experiments validate the proposed methods. It is shown that the first approach achieves a better CM noise reduction in the whole frequency ranges; on the other hand, the second approach can efficiently reduce CM noise at low frequencies and the implementation is simpler than the first approach.

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