A Generalized Common-Mode Current Cancelation Approach for Power Converters

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***Abstract*—The interwinding parasitic capacitance of transformers and the parasitic capacitance between semiconductor switches and the ground are two major contributors to the common-mode (CM) noise currents in switched mode power converters. In this paper, a generalized CM current cancelation approach is proposed for the reduction of CM noise in isolated power converters. The approach is demonstrated in a forward converter. In this approach, the total effect of the two parasitic capacitances on CM noise is represented with an equivalent parasitic capacitance (EPC) at low frequencies. With this EPC, different CM current cancelation techniques can be efficiently organized to simultaneously cancel the low-frequency CM noise caused by these two parasitic capacitances. Furthermore, the EPC can be used to evaluate and quantify the performance of CM noise reduction techniques. Both theoretical analysis and experimental results show that the proposed approach is easy to implement and can significantly attenuate low frequency CM noise and therefore greatly reduce CM filter size and cost.**

***Index Terms*—Common-mode (CM) noise, equivalent parasitic capacitance (EPC), forward converter, generalized CM current cancelation (GCMCC), parasitic capacitance.**

I. Introduction

THE size and cost of electromagnetic interference (EMI) filters are important for high-power-density and low-cost switched-mode power supply design. It is always a challenge to ensure the EMI of a converter to meet EMI standards [1]–[24]. Generally, EMI includes differential-mode (DM) noise and common-mode (CM) noise. Both CM and DM filters are used to suppress EMI. Reducing CM noise emission can greatly benefit the reduction of CM filter size and cost. In most cases, CM noise current is mainly caused by the displacement current within the interwinding parasitic capacitance of transformers and the parasitic capacitance between semiconductor switches and the ground. The CM noise paths in a forward converter are shown in Fig. 1. The CM noise current i_{CM1} flows into the ground through the parasitic capacitance between the high dv/dt nodes, such as the drain of the MOSFET S and the anode

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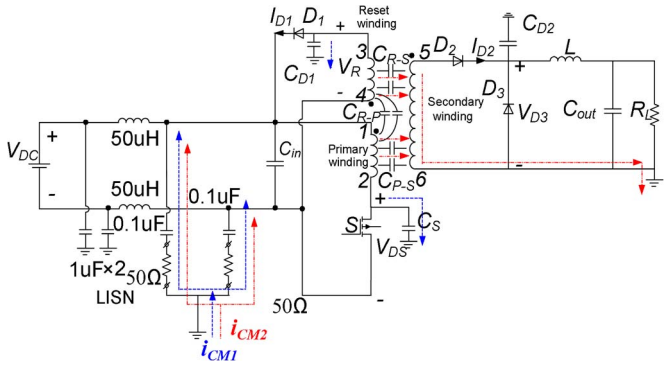

Fig. 1. CM noise paths of a forward converter.

of diode D_1, and the ground. It flows back to the converter via line impedance stabilization networks (LISNs), as shown by the blue dashed line in Fig. 1. The CM noise current i_{CM2} flows through the interwinding parasitic capacitance of the transformer to the ground. It flows back to the converter via LISNs at the primary side, as shown by the red dot dashed line in Fig. 1.

This paper first develops a CM noise model for a forward converter. In the developed model, each CM voltage source is divided to a low-frequency (LF) part and a high-frequency (HF) part. The LF parts of different CM noise voltage sources are coupled through the transformer, and they mainly contribute to LF CM noise. The CM currents flowing through the two parasitic capacitances described earlier due to the LF parts of the CM voltage sources can be represented with the product of an equivalent parasitic capacitance (EPC) value and a LF CM voltage source. These LF CM currents can be suppressed simultaneously by reducing the absolute value of the EPC. This technique is called the generalized CM current cancelation (GCMCC) in this paper. The HF parts of the CM voltage sources do not couple to each other due to the limited bandwidth of the transformer [1], and they mainly contribute to HF CM noise. Because CM filter's corner frequency is mainly decided by LF CM noise and the corner frequency determines the values and sizes of filter inductors and capacitors [19], the reduction of LF CM noise leads to a small filter size. This paper mainly focuses on the LF CM noise reduction with GCMCC. Experimental results show a significant LF CM noise reduction with GCMCC.

II. Review of Existing Techniques

While many techniques have been proposed to reduce the CM noise in power converters, most of them focus on the suppression of either the CM noise current generated by the parasitic capacitances of semiconductor switches i_{CM1} or the CM

noise current generated by the parasitic capacitance of the transformer i_{CM2} [1]–[10]. For example, in [1]–[5] and in [6]–[10], the suppression of i_{CM1} and i_{CM2} were discussed, respectively. Although the techniques in [1]–[10] can successfully attenuate either i_{CM1} or i_{CM2}, they are inefficient to cancel both i_{CM1} and i_{CM2} simultaneously. If i_{CM2} is much larger than i_{CM1}, the techniques in [1]–[5] will be quite limited, as indicated in [1]. Similarly, if i_{CM1} is dominant, the techniques in [6]–[10] are inefficient. Furthermore, in some cases, i_{CM1} and i_{CM2} can cancel each other when they are out of phase, using the techniques that can only attenuate either i_{CM1} or i_{CM2} may actually increase the total CM noise.

In [11], using double shielding layers is proposed to cancel both i_{CM1} and i_{CM2} of a flyback converter by controlling the parasitic capacitance between the two shielding layers of the transformer based on the balance concept proposed in [14] and [15]. However, inserting two shielding layers into a transformer introduces additional power loss, size, and cost, and it is hard to control the parasitic capacitance between the two shielding layers if printed circuit board (PCB) windings are not used. Furthermore, this technique is impractical in a fully interleaved transformer structure since too many shielding layers are needed. While [17] discusses the application of the general balance technique [14], [15] to a two-switch forward converter to reduce its total CM noise, it is necessary to pursue a generalized cancelation approach that can cancel both i_{CM1} and i_{CM2} simultaneously for isolated power converters.

This paper proposes the concepts of EPC and GCMCC based on a forward converter. EPC represents the total effects of the two CM parasitic capacitances on LF CM noise generation described previously for an isolated converter. If the absolute value of EPC is reduced, the LF CM noise can be attenuated. To simultaneously cancel the LF CM noise caused by the two parasitic capacitances, a methodology, i.e., GCMCC, is developed based on the expression of EPC. As a result, GCMCC is easier and more flexible to use to cancel LF CM noise than existing approaches. Furthermore, EPC can be used to quantify the performance of CM noise reduction techniques at low frequencies. Since the corner frequency of a CM filter is determined by LF CM noise and the higher the corner frequency, the smaller the filter size, GCMCC can help reduce both CM filter size and cost.

III. Analysis of CM Noise of a Forward Converter

Fig. 1 shows the topology and the CM noise paths of a forward converter. In Fig. 1, C_S is the parasitic capacitance between the drain of MOSFET and the ground, and C_{D1} is the parasitic capacitance between the anode of D_1 and the ground. The capacitors C_{R-S}, C_{P-S}, and C_{R-P}, are the interwinding parasitic capacitances of the transformer.

Fig. 2 shows the gate signal V_G, drain-to-source voltage waveform V_{DS} of the MOSFET S, current waveform I_{D1} of the diode D_1, current waveform I_{D2} of the diode D_2, and voltage waveform V_{D3} of the diode D_3. When the MOSFET S is on, the diode D_2 conducts current, and the diodes D_1 and D_3 are reverse biased. When the MOSFET S is off, D_2 stops conducting current; D_3 commutes the inductor current and current I_{D1} flows through D_1 to reset the transformer. After the transformer is fully reset, D_1 is reversely biased again.

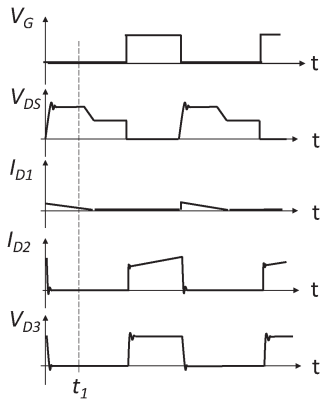

Fig. 2. Voltage and current waveforms of the forward converter in Fig. 1.

A. CM Noise Source Model of a Forward Converter

Based on substitution theory and author's previous efforts in [15], when the semiconductor switches in Fig. 1 are substituted with voltage sources or current sources, which have the same voltage or current waveforms as the original semiconductor switches, the currents and voltages in other parts of the circuit are unchanged. After the substitution, the nonlinear switches can be replaced with voltage and current sources. The effects of different noise sources on CM noise can therefore be analyzed with superposition theory. Two rules should be followed to apply the techniques to CM noise analysis.

1) The substitution should avoid voltage source loops and current source nodes because there are no unique current solution in voltage source loops and no unique voltage solution in current source nodes.
2) Although there are different substitutions available, the substitutions that are convenient for CM noise analysis are preferred.

Based on the second rule given, on the primary side, the MOSFET S is substituted with a voltage source V_{DS}, which has the same voltage waveform as the drain-to-source voltage. On the other hand, based on the first rule given, the diode D_1 cannot be substituted with a voltage source because it forms a voltage source loop with V_{DS} between the two coupled windings. Because of this, the diode D_1 is substituted with a current source I_{D1}, which has the same current waveform as the diode current.

On the secondary side, based on the two rules given, the diodes D_2 and D_3 are substituted with current source I_{D2} and voltage source V_{D3}, respectively.

Fig. 3 shows the noise model after the substitutions. It should be pointed out that the internal impedance values of voltage sources V_{DS} and V_{D3} are zero, and the internal impedance values of current sources I_{D1} and I_{D2} are infinite.

In Fig. 3, V_{DS}, V_{D3}, I_{D1}, and I_{D2} are composed of both dc and ac terms. After the ac and dc terms are decoupled, each of them still meets Kirchhoff's current law and Kirchhoff's

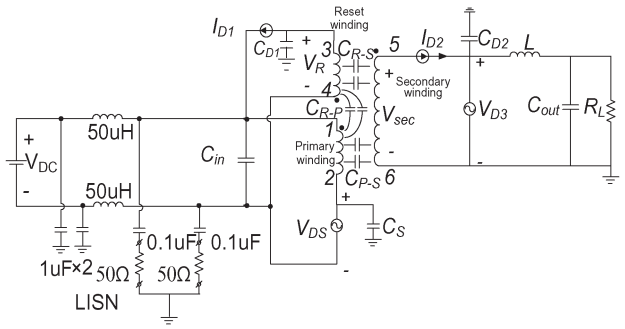

Fig. 3. Noise model for the forward converter in Fig. 1 with substitution theory applied.

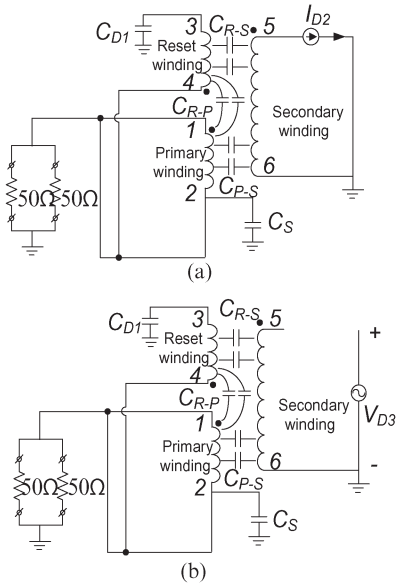

Fig. 4. CM noise due to I_{D2} and V_{D3}. (a) Effect of I_{D2} and (b) effect of V_{D3}.

voltage law. For noise analysis purpose, only the ac terms are analyzed in the following and V_{DS}, V_{D3}, I_{D1}, and I_{D2} will only represent their ac terms in the following figures and equations, except in the measurement results in Fig. 12. To develop the CM noise model for the forward converter in Fig. 1, LISNs can be approximately modeled as two 50-Ω resistors in parallel. The input capacitor $C_{\rm in}$ is a 22 μF capacitor with an equivalent series resistance of 0.6 Ω and an equivalent series inductance of 12 nH (2.26 Ω at 30 MHz). Within the conducted EMI frequency range (150 kHz-30 MHz), it can be considered short circuit since its impedance is much smaller than LISN's impedance. Furthermore, since L and $C_{\rm out}$, resistive load R_L, and the parasitic capacitance C_{D2} on the output are in parallel with the voltage source V_{D3}, they will not generate CM noise and can be removed. Finally, the effects of the noise sources can be analyzed based on superposition theorem as analyzed in [15]. Based on superposition theorem, the effect of the current source I_{D2} on CM noise can be analyzed in Fig. 4(a) with I_{D1} open, and V_{D3} and V_{DS} shorted. The effect of the voltage source V_{D3} on CM noise can be analyzed in Fig. 4(b) with V_{DS} shorted, and I_{D1} and I_{D2} open. In Fig. 4(a), it is shown that the current source I_{D2} is shorted by the secondary side of the transformer because the primary winding of the transformer

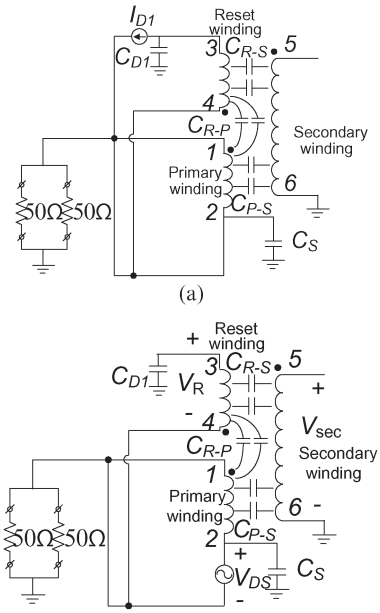

Fig. 5. CM noise due to I_{D1} and V_{DS}. (a) Effect of I_{D1} and (b) effect of V_{DS} (CM noise model of the forward converter).

is shorted. As a result, I_{D2} does not contribute to CM noise. This is true as transformer windings are well coupled at LF. In Fig. 4(b), V_{D3} will not generate CM noise either. Similarly, the effects of I_{D1} and V_{DS} are analyzed in Fig. 5(a) and (b), respectively. In Fig. 5(a), because the primary winding is shorted, the current source I_{D1} was shorted; therefore, it does not contribute to CM noise. In Fig. 5(b), V_{DS} leads to voltages $V_{\rm sec}$ on the secondary side and V_R on the reset winding. V_{DS}, $V_{\rm sec}$, and V_R contribute to CM noise via the interwinding capacitance and the parasitic capacitance C_S and C_{D1}. Because of this, Fig. 5(b) shows the CM noise model for the forward converter.

In Fig. 5(b), as the impedances of the parasitic capacitances C_{D1}, C_S, C_{P-S}, and C_{R-S} are much higher than that of LISNs within the concerned frequency range, the CM current $i_{\rm Switches}$ flowing through the parasitic capacitance C_{D1} and C_S can be estimated as

$$i_{\rm Switches} = C_S \frac{dV_{DS}}{dt} + C_{D1} \frac{dV_R}{dt}. \quad (1)$$

B. CM Current Flowing Through the Transformer

1) Parasitic Capacitance in the Transformer: Fig. 6 shows the transformer under investigation. Fig. 6(a) shows the actual transformer in the forward converter of Fig. 1, and Fig. 6(b) shows its winding structure and terminal connections. The terminal sequence numbers in Fig. 6(b) correspond to the terminal sequence numbers in Fig. 1. Two windows of the transformer are symmetric. The enlarged right window with interlayer parasitic capacitance is shown in Fig. 6(c). There are four layers in the transformer. Layer P is the primary winding, layer R is the reset winding, and layers S_1 and S_2 are the first and the second layers of the secondary winding. The parasitic capacitances include $C_{S2-\rm Core}$ between S_2 and core, C_{S1-S2} between S_1 and S_2, C_{R-S1} between R and S_1, C_{P-S1} between

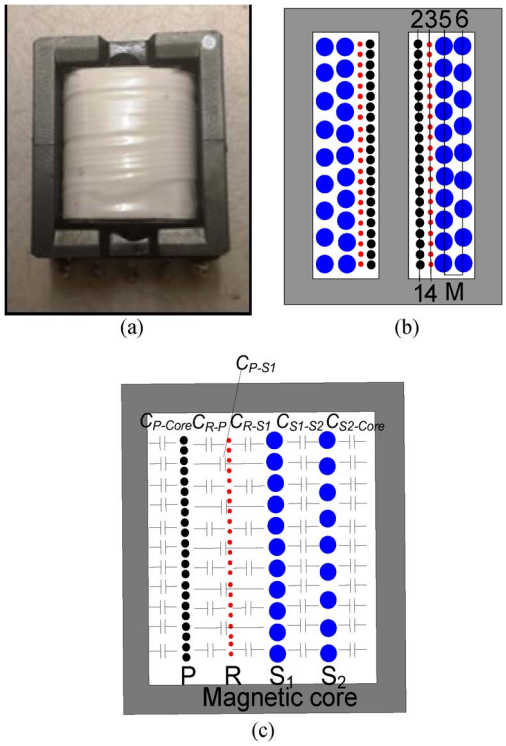

Fig. 6. Transformer under investigation. (a) Actual transformer. (b) Structure and connections. (c) Interlayer parasitic capacitance (right window).

P and S_1, C_{R-P} between R and P and $C_{P-\mathrm{Core}}$ between P and core.

In this transformer, the turn-to-turn distances of the layers P, S_1, and S_2 are very small. This effectively prevents the electric field from penetrating one of these winding layers. Because of this, it is reasonable to assume that there is no interlayer parasitic capacitance penetrating these layers. Thus, C_{R-S2} can be ignored. C_{R-S1} is to be referred to as C_{R-S} in later analysis. However, the turn-to-turn distance of layer R is much larger than those in the other layers because the reset winding wire is very thin as it carries small current only. This makes the parasitic capacitance C_{P-S1} between layers P and S_1 not ignorable. The ferrite magnetic core has high permittivity, which makes it behave similarly to a short circuit for electric field [6]; thus, $C_{P-\mathrm{Core}}$ and $C_{S2-\mathrm{Core}}$ are like directly connected. As a result, the parasitic capacitance C_{P-S2} between layers P and layer S_2 is equal to $C_{P-\mathrm{Core}}$ in series with $C_{S2-\mathrm{Core}}$.

2) CM Currents Due to the Transformer: In Fig. 1, it is shown that the interwinding parasitic capacitance C_{R-P} between the primary winding and the reset winding on the primary side is not on the paths of the CM noise. Similarly, there is no CM current flowing through interlayer capacitance C_{S1-S2} within the secondary winding. The reason is that it is in parallel with the secondary winding and the secondary winding is similar to a voltage source as the primary windings are connected to a voltage source. C_{R-P} and C_{S1-S2} will be ignored in the later analysis. On the other hand, the CM noise current generated from the identified CM voltage source can flow between primary and secondary via C_{P-S} and C_{R-S} and then flow back through the LISNs, as shown in Fig. 1. Here,

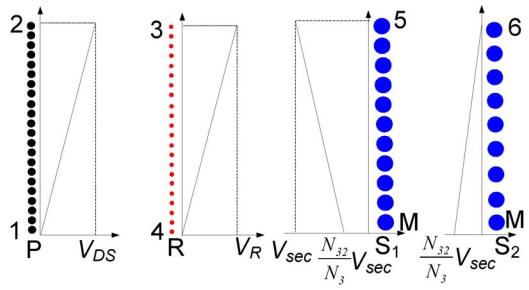

Fig. 7. Voltage potentials along winding layers.

C_{P-S} includes both C_{P-S1} and C_{P-S2} in Fig. 6(c), and C_{R-S} equals to C_{R-S1}.

For the winding terminal arrangement shown in Fig. 6(b), the voltage potentials along winding layers P, R, S_1 and S_2 in the right window corresponding to the time instant t_1 in Fig. 2 after dc biases are removed, are plotted in Fig. 7. It is assumed that the voltage potentials are evenly distributed along the windings. The voltages of layers P, R, S_1 and S_2 vary with time as shown in Fig. 2. Fig. 7 is just a general example, and the derived equations can be applied to any time instant in Fig. 2.

In Fig. 7, N_{32} is the number of turns of layer S_2. It is assumed that the parasitic capacitance is evenly distributed between two layers, and the voltage across LISNs is ignored for the same reason as used for (1) in Section III-A. The displacement current i_{P-S1} between layers P and S_1 can be expressed as

$$i_{P-S1} = \frac{C_{P-S1}}{2}\frac{d}{dt}\left(V_{DS} - V_{\mathrm{sec}} - \frac{N_{32}}{N_3}V_{\mathrm{sec}}\right). \quad (2)$$

Similarly, the displacement current between layers R and S_1, i_{R-S1}, and the displacement current between layers P and S_2, i_{P-S2}, can be expressed as

$$i_{R-S1} = \frac{C_{R-S1}}{2}\frac{d}{dt}\left(V_R - V_{\mathrm{sec}} - \frac{N_{32}}{N_3}V_{\mathrm{sec}}\right) \quad (3)$$

$$i_{P-S2} = \frac{C_{P-S2}}{2}\frac{d}{dt}\left(V_{DS} - \frac{N_{32}}{N_3}V_{\mathrm{sec}}\right). \quad (4)$$

Then, the CM current i_{Trans} flowing through the parasitic capacitance of the transformer is

$$i_{\mathrm{Trans}} = i_{P-S1} + i_{R-S1} + i_{P-S2}. \quad (5)$$

C. Total CM Current of the Forward Converter

For the forward converter, its total CM current is the sum of the CM currents through the parasitic capacitance C_S and C_{D1} and the CM current through the transformer, i.e.,

$$i_{\mathrm{CM}} = i_{\mathrm{Switches}} + i_{\mathrm{Trans}}. \quad (6)$$

Due to the presence of the transformer's leakage inductance, parasitic inductance of traces, parasitic capacitance of the transformer, and parasitic capacitance between the two ends of semiconductor switches, the CM voltages in Fig. 5(b) have HF ringing. Due to the limited bandwidth of the transformer, the LF parts of the CM voltages are well coupled, but the HF parts of the CM voltages are not well coupled [1]. Based on this, the

CM voltages V_{DS}, V_R, and $V_{\rm sec}$ can be divided into coupled LF parts, V_{DS_C}, V_{R_C}, and $V_{\rm sec\_C}$ and uncoupled HF parts V_{DS_NC}, V_{R_NC} and $V_{\rm sec\_NC}$. The coupled LF parts V_{DS_C}, V_{R_C}, and $V_{\rm sec\_C}$ mainly contribute to LF CM noise and the uncoupled HF parts V_{DS_NC}, V_{R_NC} and $V_{\rm sec\_NC}$ mainly contribute to HF CM noise. The two parts meet the conditions in the following:

$$V_{DS} = V_{DS\_C} + V_{DS\_NC} \tag{7}$$
$$V_R = V_{R\_C} + V_{R\_NC} \tag{8}$$
$$V_{\rm sec} = V_{\rm sec\_C} + V_{\rm sec\_NC}. \tag{9}$$

For the LF parts, if the transformer's turns ratio between primary winding, reset winding, and secondary winding is $N_1 : N_2 : N_3$, the relationships between V_{DS_C}, V_{R_C}, and $V_{\rm sec\_C}$ are

$$\frac{V_{DS\_C}}{V_{R\_C}} = \frac{N_1}{N_2} \tag{10}$$
$$\frac{V_{DS\_C}}{V_{\rm sec\_C}} = -\frac{N_1}{N_3}. \tag{11}$$

Based on equations from (1) to (11), the total CM current can be expressed as (12), shown at the bottom of the page, where

$$\begin{aligned} C_{\rm eq} = {} & C_S + \frac{C_{P-S1} + C_{P-S2}}{2} \\ & + \left(C_{D1} + \frac{C_{R-S1}}{2}\right)\frac{N_2}{N_1} \\ & + \frac{C_{P-S1} + C_{R-S1}}{2}\left(\frac{N_{32}}{N_3} + 1\right)\frac{N_3}{N_1} \\ & + \frac{C_{P-S2}N_{32}}{2N_1} \end{aligned} \tag{13}$$
$$C_{\rm HF\_DS} = C_S + \frac{C_{P-S1} + C_{P-S2}}{2} \tag{14}$$
$$C_{\rm HF\_D1} = C_{D1} + \frac{C_{R-S1}}{2} \tag{15}$$
$$C_{\rm HF\_sec} = \frac{C_{P-S1} + C_{R-S1}}{2}\left(\frac{N_{32}}{N_3} + 1\right) + \frac{C_{P-S2}N_{32}}{2N_3}. \tag{16}$$

In the given equations, the LF CM noise from all parasitic capacitances of the forward converter due to V_{DS_C}, V_{R_C}, and $V_{\rm sec\_C}$ is equivalent to the CM noise generated from an EPC $C_{\rm eq}$ between the drain of the MOSFET and the ground. The $C_{\rm eq}$ could be positive or negative in different cases. The smaller the absolute value of EPC is, the lower the LF CM noise $i_{\rm CM\_LF}$ is. EPC can also be lumped to other locations such as between the anode of diode D_1 and the ground or between terminal 5 of the transformer and any node with constant voltage potential on the primary side. The following discussion is based on the EPC between the drain of the MOSFET and the ground. Since the HF parts of the CM voltage sources, V_{DS_NC}, V_{R_NC} and $V_{\rm sec\_NC}$ do not meet (10) and (11), the effect of parasitic capacitances due to V_{DS_NC}, V_{R_NC}, and $V_{\rm sec\_NC}$ can only be represented with separated capacitances $C_{\rm HF\_DS}$, $C_{\rm HF\_D1}$, and $C_{\rm HF\_sec}$.

IV. CM Noise Cancelation Techniques

Based on (12), the LF CM noise emission due to V_{DS_C}, V_{R_C} and $V_{\rm sec\_C}$ can be attenuated by reducing the absolute value of $C_{\rm eq}$. As long as the absolute value of $C_{\rm eq}$ is reduced, the LF CM noise will be reduced, as well as the filter size and cost. In (12), the CM noise generated by V_{DS_NC}, V_{R_NC}, and $V_{\rm sec\_NC}$ cannot be reduced with reduced EPC; therefore, other techniques have to be employed. This paper mainly focuses on the LF CM noise cancelation by reducing the absolute value of EPC. This technique is GCMCC.

Compared with existing techniques, GCMCC can be used to optimize and organize different techniques to reduce EPC to reduce LF CM noise. It can suppress $i_{\rm Switches}$ and $i_{\rm Trans}$ simultaneously and is easier and more flexible. It can be applied to other isolated converters following a similar procedure.

A. Optimization of Converter Configuration

Fig. 8(a) shows another forward converter configuration. Its reset diode D_1 has a different position from that in Fig. 1. This small difference does not affect the operation of the forward converter, but it may significantly affect CM noise.

In Fig. 8(a), the reference direction of V_R is different from that in Fig. 1, C'_{D1} is the parasitic capacitance between the cathode of D_1 and the ground and the other parameters are the same as those in Fig. 1. For this configuration, the CM noise model is Fig. 8(b), and the following relationships are satisfied:

$$\frac{V_{DS\_C}}{V_{R\_C}} = -\frac{N_1}{N_2} \tag{17}$$
$$i_{\rm Switches} = C_S\frac{dV_{DS}}{dt} + C'_{D1}\frac{dV_R}{dt}. \tag{18}$$

Although the voltage distributions within transformer windings are different from those shown in Fig. 7, following the same procedure as in Section III-B, the displacement current between any two layers across the primary side and secondary side can still be expressed as (2)–(4). Then, based on (2)–(9), (11), (17), and (18), the EPC $C_{\rm eq1}$ for the configuration shown in Fig. 8(a) can be derived as

$$\begin{aligned} C_{\rm eq1} = {} & C_S + \frac{C_{P-S1} + C_{P-S2}}{2} - \left(C'_{D1} + \frac{C_{R-S1}}{2}\right)\frac{N_2}{N_1} \\ & + \frac{C_{P-S1} + C_{R-S1}}{2}\left(\frac{N_{32}}{N_3} + 1\right)\frac{N_3}{N_1} + \frac{C_{P-S2}N_{32}}{2N_1}. \end{aligned} \tag{19}$$

$$\begin{aligned} i_{\rm CM} = {} & \underbrace{\left(C_{\rm eq}\frac{dV_{DS\_C}}{dt}\right)}_{\rm LF} + \underbrace{\left(C_{\rm HF\_DS}\frac{dV_{DS\_NC}}{dt} + C_{\rm HF\_D1}\frac{dV_{R\_NC}}{dt} - C_{\rm HF\_sec}\frac{dV_{\rm sec\_NC}}{dt}\right)}_{\rm HF} \\ = {} & i_{\rm CM\_LF} + i_{\rm CM\_HF} \end{aligned} \tag{12}$$

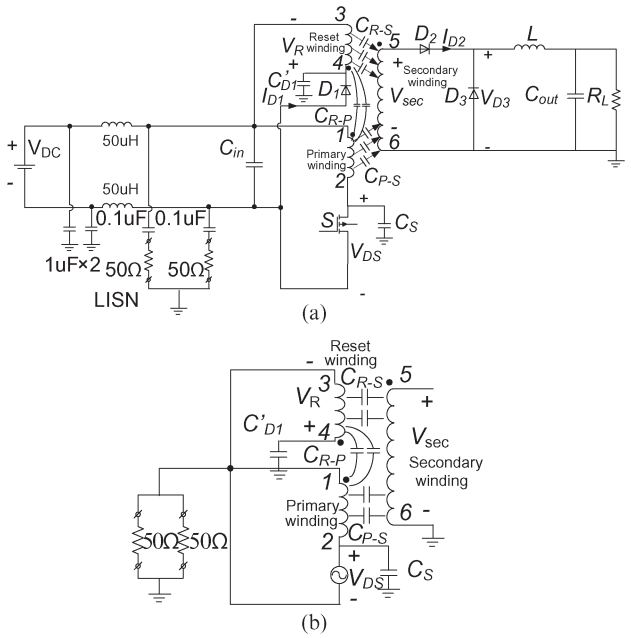

Fig. 8. Different forward converter circuit configuration: (a) Circuit and (b) CM noise model.

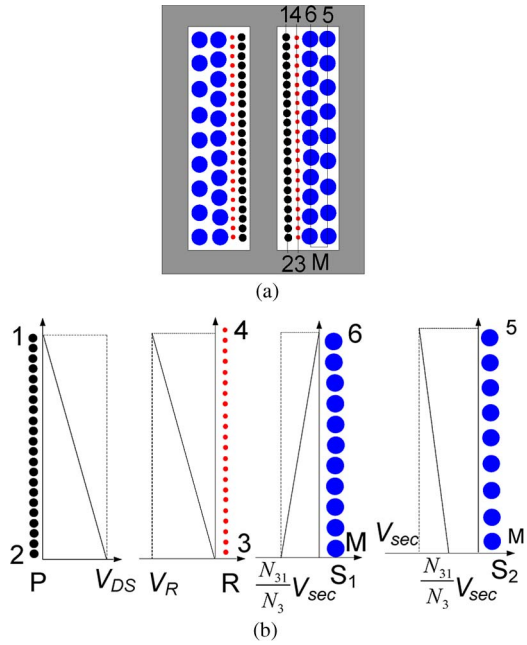

Fig. 9. (a) Modified transformer terminal connections and (b) voltage potentials along winding layers with the modified transformer terminal connections.

If C_{eq1} is smaller than C_{eq}, then the configuration in Fig. 8(a) gives lower LF CM noise than that in Fig. 1. The same rule applies to the CM noise analysis in other cases.

B. Design of Transformer Winding Terminal Connections

It was discussed in [6] and [17] that different transformer terminal arrangements influence the CM noise flowing through the interwinding parasitic capacitances of the transformer. However, these papers do not give specific and systematic rules for an efficient transformer winding terminal connection design. According to GCMCC developed in this paper, the basic rule to design transformer winding terminal connections is to make the absolute value of the converter's EPC C_{eq} as small as possible.

For the forward converter with the configuration in Fig. 8(a), when its transformer's terminal connections are reversed to Fig. 9(a), the voltage distributions within transformer windings change to Fig. 9(b). In Fig. 9(b), N_{31} is the turn number of the first layer of the secondary winding S_1. It equals to $(N_3 - N_{32})$. The displacement currents between any two layers across the primary and secondary sides change to

$$i_{P-S1} = \frac{C_{P-S1}}{2}\frac{d}{dt}\left(V_{DS} - \frac{N_{31}}{N_3}V_{\text{sec}}\right) \tag{20}$$

$$i_{R-S1} = \frac{C_{R-S1}}{2}\frac{d}{dt}\left(V_R - \frac{N_{31}}{N_3}V_{\text{sec}}\right) \tag{21}$$

$$i_{P-S2} = \frac{C_{P-S2}}{2}\frac{d}{dt}\left(V_{DS} - V_{\text{sec}} - \frac{N_{31}}{N_3}V_{\text{sec}}\right). \tag{22}$$

Based on (5)–(9), (11), (17), (18), and (20)–(22), the EPC C_{eq2} in this case is

$$C_{\text{eq2}} = C_S + \frac{C_{P-S1} + C_{P-S2}}{2} - \left(C'_{D1} + \frac{C_{R-S1}}{2}\right)\frac{N_2}{N_1} + \frac{C_{P-S1} + C_{R-S1}}{2}\frac{N_{31}}{N_1} + \frac{C_{P-S2}N_3}{2N_1}\left(\frac{N_{31}}{N_3} + 1\right). \tag{23}$$

A better transformer terminal connection can be selected for LF CM noise attenuation based on the absolute values of C_{eq1} and C_{eq2}.

C. Design of External Cancellation Capacitors

Another technique to reduce LF CM noise is to add an external cancelation capacitor. While several papers have presented this technique [1, 2], they only focus on reducing the CM noise due to C_S, which is inefficient and may even increase the total CM noise when applied to isolated converters, as discussed earlier. With the proposed GCMCC, the external capacitor is designed based on the value of EPC. It minimizes CM noise in the LF range.

For the forward converter with the configuration in Fig. 8(a), when its EPC is positive, a cancelation capacitor C_{add} can be added in parallel with the parasitic capacitance C'_{D1} between the cathode of the diode D_1 and the ground, as shown in Fig. 10. The total LF CM current flowing through the EPC and the added external capacitor needs to be zero, i.e.,

$$i_{\text{CM\_LF}} = C_{\text{eq}}\frac{dV_{DS\_C}}{dt} + C_{\text{add}}\frac{dV_{R\_C}}{dt} = 0. \tag{24}$$

From (17) and (24), C_{add} is equal to $C_{\text{eq}}N_1/N_2$. C_{add} can also be added between terminal 5 and the ground with a value equal to $C_{\text{eq}}N_1/N_3$. When the EPC is negative, C_{add} can be calculated similarly, and it should be in parallel with C_S.

D. Discussion

In this section, three CM noise reduction techniques are investigated based on the proposed EPC and GCMCC. Compared with existing techniques that focus on the reduction of

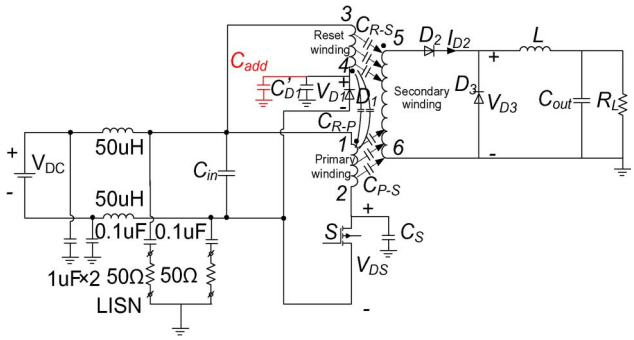

Fig. 10. Design of external cancelation capacitor when $C_{\rm eq}$ is positive.

either $i_{\rm CM1}$ or $i_{\rm CM2}$, GCMCC focuses on the reduction of total CM noise. It is therefore more efficient and more flexible. To efficiently apply the three techniques given, the LF CM noise should be first reduced from the CM noise source side. This means to select an optimal power converter configuration and an optimal transformer terminal connection in the first two steps. The design of the external cancelation capacitor based on EPC can then be applied in the third step.

V. Experimental Results

To evaluate the effectiveness of GCMCC, experiments were conducted on the forward converter in Fig. 1. $V_{\rm DC}$ is 48 V; output voltage is 12 V, and output power is 36 W. The transformer's winding structure is shown in Fig. 6(b). The switching frequency is 100 kHz. The parasitic capacitance of the semiconductor devices and that of the transformer are first measured with an Agilent 4395 impedance analyzer. Based on the measurement results, experiments are carried out to validate the GCMCC technique.

A. Parasitic Capacitance Measurement

In the prototype, the drain of the MOSFET is directly soldered to a large piece of PCB copper for heat dissipation, which results in a large C_S. To accurately measure C_S, all the components affecting the measurement of C_S, including the transformer, are disconnected. The measured C_S is about 10 pF. The measured parasitic capacitances C_{D1} and C'_{D1} are less than 1 pF. Their contribution to EPC is very small with turns ratio considered; therefore, they are ignored in later analysis.

For the transformer, the primary winding has 22 turns; the reset winding has 22 turns, and the secondary winding has 20 turns. The first layer and the second layer of the secondary winding are 11 and 9 turns, respectively. The wire is #AWG22 for the primary winding, #AWG32 for the reset winding, and two #AWG22 in parallel for the secondary winding. The material of the ferrite core is MnZn, and its permeability is 2250. To eliminate the effects of the parasitic capacitance and the voltage gradients within one winding on interwinding capacitance measurement, the two terminals of each winding are shorted, which leads to an equal voltage potential within each winding. If the three windings are represented with points P, R, and S, the three parasitic capacitance, C_{R-P}, C_{P-S}, and C_{R-S}, between any two windings of the transformer, have an equivalent circuit

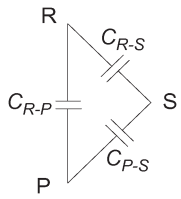

Fig. 11. Equivalent connections of C_{R-P}, C_{P-S}, and C_{R-S}.

TABLE I
C_{P-S}, C_{R-S} AND C_{R-P} UNDER DIFFERENT CONDITIONS

	$C_{P\text{-}S}$	$C_{R\text{-}P}$	$C_{R\text{-}S}$
Full Transformer	13 pF	47 pF	62 pF
Transformer without magnetic core	11 pF	46.5 pF	61 pF
Transformer without magnetic core and S_2	11 pF	46 pF	61 pF

shown in Fig. 11. The parasitic capacitance cannot be directly measured since all of them are always connected; however, the parasitic capacitance can be calculated based on Fig. 11 and the measured impedance between any two windings.

In Fig. 11, the capacitances C_{MR-P} between R and P, C_{MP-S} between P and S, and C_{MR-S} between R and S are first measured. The capacitances C_{R-P}, C_{P-S}, and C_{R-S} can be solved from the following based on Fig. 11:

$$C_{MR-P} = C_{R-P} + \frac{C_{P-S}C_{R-S}}{C_{P-S}+C_{R-S}} \tag{25}$$

$$C_{MP-S} = C_{P-S} + \frac{C_{R-P}C_{R-S}}{C_{R-P}+C_{R-S}} \tag{26}$$

$$C_{MR-S} = C_{R-S} + \frac{C_{R-P}C_{P-S}}{C_{R-P}+C_{P-S}}. \tag{27}$$

As discussed in Section III, C_{P-S} is composed of C_{P-S1} and C_{P-S2}, and the layers P and S_1 have a shielding effect to layers R and S_2, which makes the parasitic capacitance between layers R and S_2 ignorable. To verify the shielding effect of layers P and S_1 to electric field and quantify C_{P-S1}, C_{P-S2}, and C_{R-S}, measurements are conducted for three cases: full transformer, transformer without magnetic core, and transformer without both magnetic core and layer S_2. The parasitic capacitances C_{P-S}, C_{R-S}, and C_{R-P} calculated from the measurement results are summarized in Table I.

In Table I, after the magnetic core is removed, C_{P-S2} is eliminated; therefore, the calculated result of C_{P-S} only includes C_{P-S1}. From Table I, the C_{P-S} of the full transformer is 13 pF, and the C_{P-S} of the transformer without magnetic core is 11 pF. Thus, C_{P-S1} and C_{P-S2} are 11 and 2 pF, respectively. The measurement results in Table I also show that C_{P-S}, C_{R-S}, and C_{R-P} of the transformer without magnetic core and the C_{P-S}, C_{R-S}, and C_{R-P} of the transformer without both magnetic core and layer S_2 are almost the same, which verifies the shielding effect of layers P and S_1. Thus, it is reasonable to ignore C_{R-S2}, and in this case, C_{R-S} is equal to C_{R-S1}. Several transformers with the same model number are measured, and their parasitic capacitances are very close;

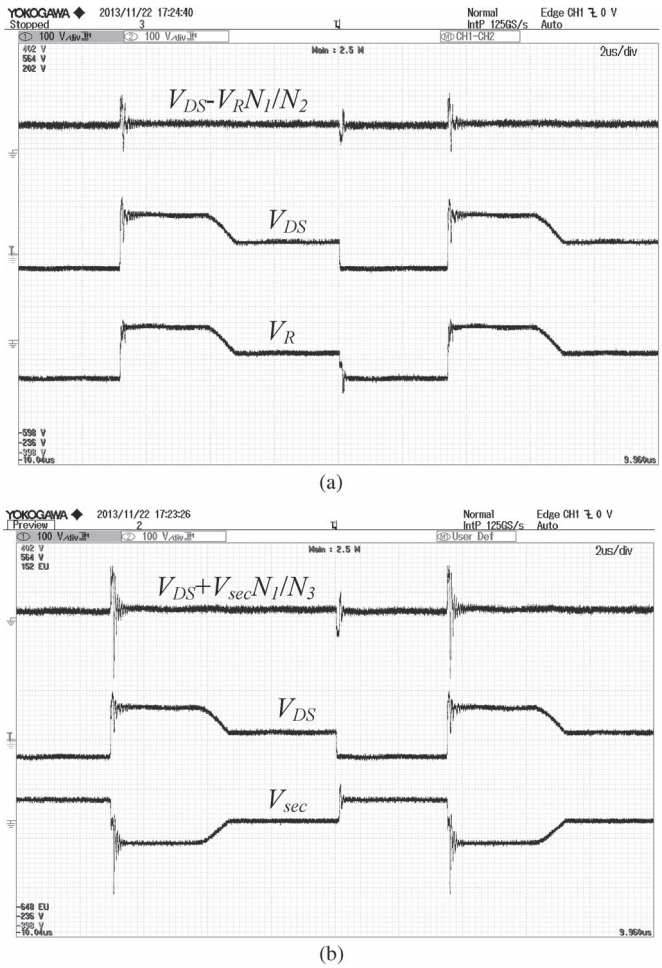

Fig. 12. LF CM voltages are coupled but HF CM voltages are not: (a) V_{DS}, V_R, and $V_{DS} - V_R N_1/N_2$ and (b) V_{DS}, $V_{\rm sec}$, and $V_{DS} + V_{\rm sec} N_1/N_3$.

therefore, in the following experiments, the C_{P-S1}, C_{P-S2}, C_{R-S} (or C_{R-S1}) obtained based on Table I will be used. They are 11, 2, and 61 pF, respectively.

B. Coupling of LF and HF CM Noise Voltages

For the original converter in Fig. 1 and the transformer structure and connection in Fig. 6(b), the waveforms of V_{DS}, V_R, $V_{\rm sec}$, $V_{DS} - V_R N_1/N_2$, and $V_{DS} + V_{\rm sec} N_1/N_3$ are shown in Fig. 12. As analyzed previously, V_{DS}, V_R, and $V_{\rm sec}$ are composed of LF parts V_{DS_C}, V_{R_C}, and $V_{{\rm sec}\_C}$ and HF parts V_{DS_NC}, V_{R_NC}, and $V_{{\rm sec}\_NC}$. Since the LF parts V_{DS_C}, V_{R_C}, and $V_{{\rm sec}\_C}$ are coupled through the transformer and proportional to each other as indicated in (10) and (11), they will cancel each other in terms of $V_{DS} - V_R N_1/N_2$ and $V_{DS} + V_{\rm sec} N_1/N_3$. However, the HF parts V_{DS_NC}, V_{R_NC}, and $V_{{\rm sec}\_NC}$ do not couple to each other and cannot be canceled in terms of $V_{DS} - V_R N_1/N_2$ and $V_{DS} + V_{\rm sec} N_1/N_3$. From Fig. 12, $V_{DS} - V_R N_1/N_2$ and $V_{DS} + V_{\rm sec} N_1/N_3$ are dc (represent cancelation) superposed with high-frequency ringing (represent no cancelation), which verifies the analysis given. Based on the measurement results, the EPC $C_{\rm eq}$ is calculated as 95 pF.

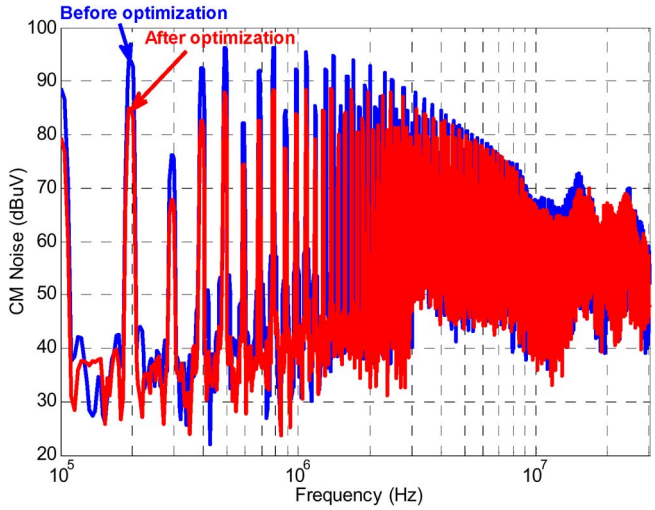

Fig. 13. CM noise comparison before and after reset diode optimization.

C. Experimental Verification

1) Optimization of Converter Configuration: As discussed in Section IV, for the original forward converter in Fig. 1, when the reset diode is moved to the pin 4 of the transformer as shown in Fig. 8(a), its CM noise may be greatly reduced. Based on the measured parasitic capacitances and (13) and (19), this modification can reduce the EPC from 95 to 34 pF, a 9-dB reduction in capacitance, which leads to a 9-dB LF CM noise reduction as described in (12). In Fig. 13, the measured CM noise before and after reset diode optimization shows that up to 9-dB CM noise reduction is achieved below 5 MHz. At the same time, HF CM noise is almost unchanged. This agrees with the previous analysis.

2) Design of Transformer Winding Connections: Based on Section IV, the optimization of transformer's winding terminal connections can also reduce the CM noise. After the converter configuration is optimized from Fig. 1 to Fig. 8(a), its CM noise can be further reduced when the transformer's terminal connections are changed from Fig. 6(b) to Fig. 9(a). Based on (19) and (23), the EPC can be reduced from 34 to 5 pF, a 17-dB reduction on EPC. It means the LF CM noise can be further reduced by 17 dB via reversing the transformer's terminal connections. Fig. 14 shows the measured CM noise for the forward converter with the transformer's terminal connections in Fig. 6(b) and in Fig. 9(a). There is up to 16-dB LF CM noise reduction below 9 MHz.

3) Design of External Cancelation Capacitor:

a) Before the Transformer Terminal Connection Optimization: After the optimization of the reset diode position, the modified configuration becomes Fig. 8(a). If the CM noise is suppressed based on existing literature [1], a 10-pF cancelation capacitor will be added in parallel with C'_{D1} to cancel the LF CM noise generated by V_{DS_C} through C_S. However, the parasitic capacitance of the transformer is not included in this method. Because of this, with this 10-pF cancelation capacitor, there is still 24 pF EPC not canceled. This leads to a very limited LF CM noise reduction. The reduction is only approximate 3 dB, 20log(34 pF/24 pF).

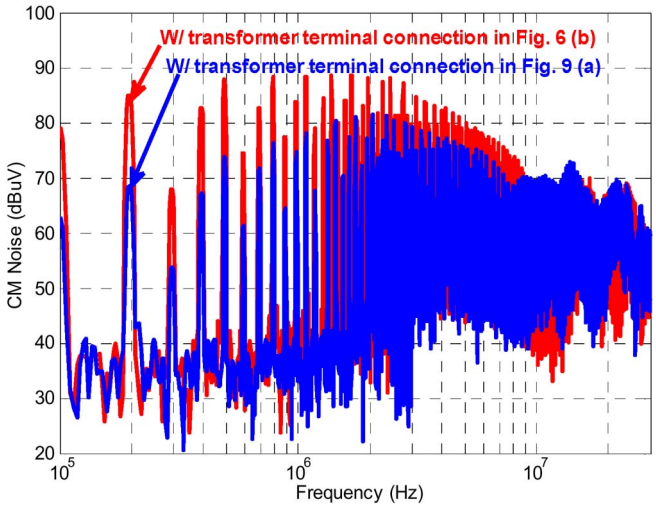

Fig. 14. CM noise comparison of the forward converter with different transformer winding terminal connections.

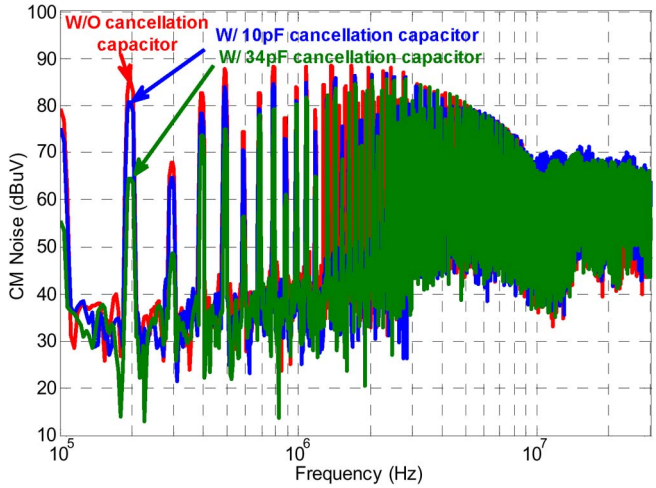

Fig. 15. CM noise of the forward converter in Fig. 8(a) without cancelation capacitor, with 10-pF cancelation capacitor based on existing literature, and with 34-pF cancelation capacitor based on GCMCC.

Based on GCMCC in Section IV, a 34-pF capacitor should be paralleled with C'_{D1} to cancel the LF CM noises generated by V_{DS_C}, V_{R_C}, and V_{sec_C} through both the parasitic capacitances of the transformer and the parasitic capacitances between semiconductor switches and the ground. Fig. 15 shows the comparison of the CM noise without cancelation capacitor, with 10-pF cancelation capacitor and with 34-pF cancelation capacitor after the reset diode position is optimized. It is shown that the conventional cancelation method has only around 3-dB reduction, whereas the proposed GCMCC can further reduce the LF CM noise by 15 dB.

It should be pointed that the CM noise will be over canceled when the external cancelation capacitor is greater than 34 pF. The EPC will be negative, and the LF CM noise will be higher than that with 34 pF capacitor. Fig. 16 shows the measurement results when the external capacitor increases to 37 and 40 pF, which agrees with the analysis.

b) After the Transformer Terminal Connection Optimization: After the optimization of the transformer winding connections, there is still a 5-pF equivalent capacitance between the drain of MOSFET and the ground. A 5-pF capacitor was paralleled with C'_{D1} to further reduce the LF CM noise. The CM noise with and without the 5-pF capacitor are shown in Fig. 17. The LF CM noise is further reduced by 18 dB.

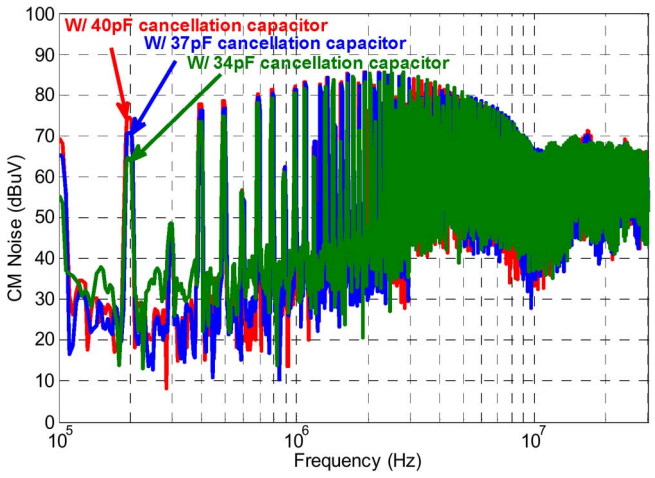

Fig. 16. Increase of CM noise due to over cancelation.

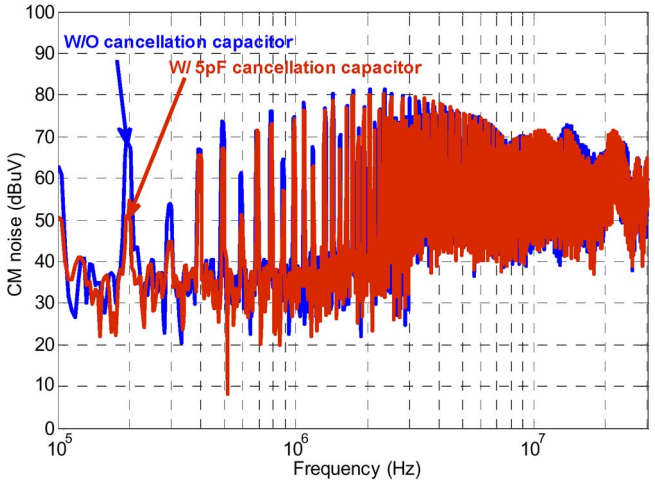

Fig. 17. CM noise with and without cancelation capacitor after the optimization of transformer winding connections.

It is shown in Fig. 15 and Fig. 17 that applying cancelation capacitor with the optimization of transformer winding connections can further reduce the LF CM noise by up to 13 dB compared with applying cancelation capacitor only. This shows that applying cancelation techniques based on the proposed GCMCC can achieve a better cancelation.

As analyzed previously, when the external capacitor increases from 5 to 7 and 10 pF, the LF CM noise also increases due to over cancelations. The measurement results are shown in Fig. 18, which also agrees with the analysis.

4) Discussion: As analyzed in Section III-C, the reason that EPC can be used to represent all the parasitic capacitances of the forward converter in the LF range is that the LF part of V_{DS}, V_R, and V_{sec} are coupled through the transformer and proportional to each other, as indicated in (10), (11), and (17). As a result, the upper frequency for the proposed technique is decided by the upper frequency of transformer's bandwidth.

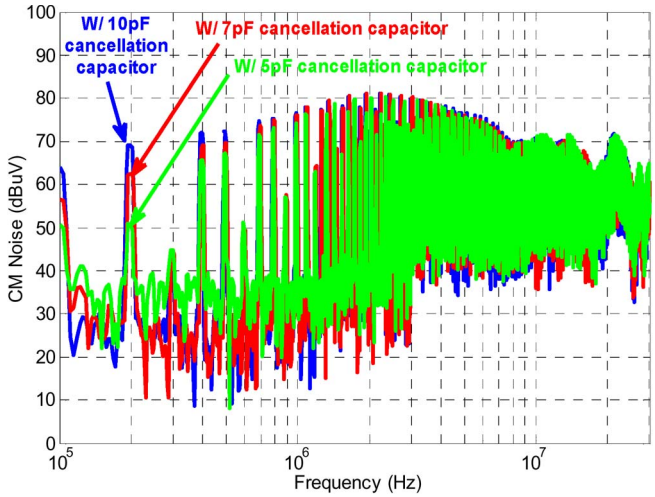

Fig. 18. Increase in CM noise due to over cancelation.

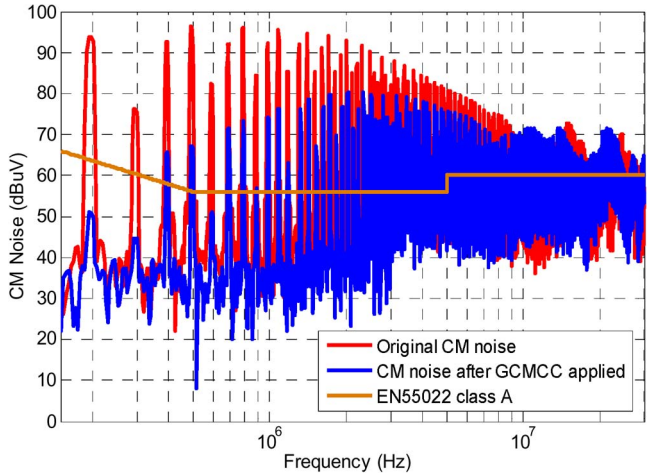

Fig. 19. Comparison of the original CM noise and the CM noise after GCMCC applied.

The closer the transformer's windings are coupled, the higher the upper frequency of the transformer's bandwidth and the upper efficient frequency of GCMCC are. In the case discussed in this paper, the efficient frequency is up to 2 MHz.

As described in (12), although GCMCC is used to attenuate LF CM noise, the high-frequency CM noise could be changed due to the change of high frequency capacitance $C_{\mathrm{HF\_}DS}$, $C_{\mathrm{HF\_}D1}$, and $C_{\mathrm{HF\_sec}}$ or the HF parts of the CM voltage sources V_{DS}, V_R, and V_{sec} due to the change of circuit and winding configurations. For example, when the transformer's terminal connections are changed from Fig. 6(b) to Fig. 9(a), its leakage inductance is changed. As a result, the high-frequency ringing of the CM voltage sources V_{DS}, V_R, and V_{sec} increases a little bit, as well as the high frequency CM noise, as shown in Fig. 14. Although GCMCC may slightly increase HF CM noise, it is insignificant compared with the LF CM noise reduction, as shown in Figs. 13, –18.

The parasitic capacitances were measured for several transformers and semiconductor devices. The average values were used to reduce the effects of parameter variations. In a practical application, the proposed technique can be used to determine an approximate capacitance and the final best external capacitance can be obtained with a small adjustment in experiments.

D. Expected EMI Filter Size Reduction

Fig. 19 shows the comparison of the CM noise of the original converter and the final CM noise after GCMCC is applied. The EMI standard EN55022 class A is also shown in Fig. 19. The CM noise attenuation requirement can be obtained in (28)

$$(V_{\mathrm{req,CM}})_{\mathrm{dB}} = (V_{\mathrm{measured,CM}})_{\mathrm{dB}} - (V_{\mathrm{limit}})_{\mathrm{dB}} + 6\ \mathrm{dB}. \quad (28)$$

The 6 dB is needed since the EMI standard is for total EMI noise, which is the vector sum of CM and DM noise.

The calculated attenuation requirements for both CM noise are shown in Fig. 20. The CM insertion loss of a one-stage LC CM filter and a two-stage $LCLC$ CM filter is 40 and 80 dB/dec,

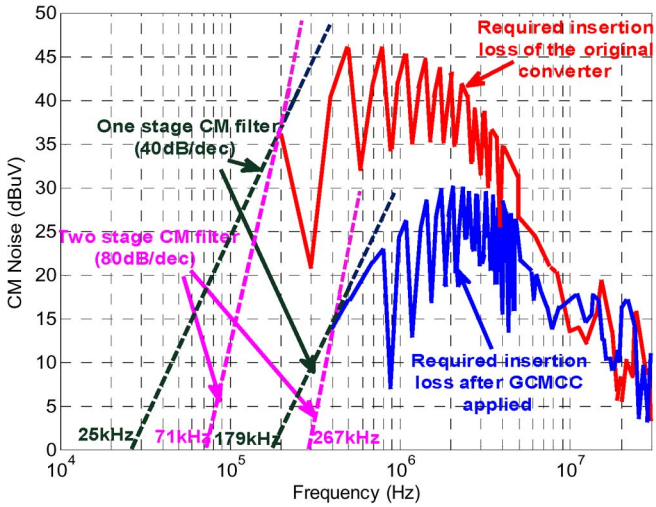

Fig. 20. Required insertion losses of CM filters for the original converter and for the converter after GCMCC applied.

respectively. Thus, a 40-dB/dec line and an 80-dB/dec line can be used to determine the corner frequencies for both one-stage LC CM filters and two-stage $LCLC$ CM filters [19]. As shown in Fig. 20, for the original converter, the corner frequencies of a one-stage LC CM filter and a two-stage $LCLC$ CM filter are 25 and 71 kHz, respectively. After GCMCC is applied, the corner frequencies increase to 179 and 267 kHz, respectively. If the filters have identical L and C in each stage, the corner frequency of the CM filter approximately meets the condition

$$f_{\mathrm{corner}} \propto \frac{1}{\sqrt{LC}}. \quad (29)$$

When f_{corner} is increased, L and C are reduced, i.e., the filter size is reduced. If the size of L and C is proportional to their values, when GCMCC is applied, the size of a one-stage LC CM filter and a two-stage $LCLC$ CM filter can be approximately reduced by 86% and 74%, respectively.

VI. Conclusion

In this paper, the concepts of EPC and GCMCC have been proposed and successfully implemented in a forward converter. The CM noise model of the forward converter was first derived. Based on the model, the parasitic capacitance between semiconductor switches and the ground, and the interwinding parasitic capacitance of transformers are modeled with an EPC. The proposed EPC can represent the effects of all the CM parasitic capacitances of the converter on the LF CM noise. The GCMCC is used to reduce the absolute value of EPC to reduce LF CM noise and EMI filter size. Compared with existing techniques, GCMCC efficiently organizes different CM noise reduction techniques to reduce the CM noise generated by the parasitic capacitance between semiconductor switches and ground, and the CM noise generated by the interwinding parasitic capacitance of transformers simultaneously. GCMCC is easy to implement, is flexible, and can achieve a good LF CM cancelation. This technique can also be applied to other converter topologies.

References

[1] D. Cochrane, D. Y. Chen, and D. Boroyevic, "Passive cancellation of common-mode noise in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 756–763, May 2003.

[2] Schmidt *et al.*, "Important aspects on effective common mode noise filtering by means of passive cancellation," in *Proc. IEEE APEC*, 2013, pp. 591–596.

[3] H. Chen, C. Chen, and Y. Ren, "Modeling and characterization of incomplete shielding effect of GND on common-mode EMI of a power converter," *IEEE Trans. Electromagn. Compat.*, vol. 53, no. 3, pp. 676–683, Aug. 2011.

[4] X. Gong, Ferreira, and J. A. , "Investigation of conducted EMI in SiC JFET inverters using separated heat sinks," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 115–125, Jan. 2014.

[5] S. Wang and F. C. Lee, "Analysis and applications of parasitic capacitance cancellation techniques for EMI suppression," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3109–3117, Sep. 2010.

[6] P. Kong and F. C. Lee, "Transformer structure and its effects on common mode EMI noise in isolated power converters," in *Proc. IEEE APEC*, 2010, pp. 1424–1429.

[7] D. Fu, S. Wang, P. Kong, F. C. Lee, and D. Huang, "Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4968–4977, Nov. 2013.

[8] Y. P. Chan, B. M. H. Pong, N. K. Poon, J. C. P. Liu *et al.*, "Common-mode noise cancellation in switching-mode power supplies using an equipotential transformer modeling technique," *IEEE Tran. Electromagn. Compat.*, vol. 54, no. 3, pp. 594–602, Jun. 2012.

[9] Z. Lu and W. Chen, "Common mode EMI noise reduction technique by noise path configuration of HF power transformer," in *Proc. IEEE IPEMC*, 2009, pp. 954–956.

[10] M. Pahlevaninezhad, D. Hamza, and P. K. Jain, "An improved layout strategy for common-mode EMI suppression applicable to high-frequency planar transformers in high-power DC/DC converters used for electric vehicles," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1211–1228, Mar. 2014.

[11] Y. Yang, D. Huang, F. C. Lee, and Q. Li, "Transformer shielding technique for common mode noise reduction in isolated converters," in *Proc. IEEE ECCE*, 2013, pp. 4149–4153.

[12] Y. Y. Maillet *et al.*, "High-density EMI filter design for DC-Fed motor drives," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1163–1172, May 2010.

[13] S. Wang and F. C. Lee, "Common-mode noise reduction for power factor correction circuit with parasitic capacitance cancellation," *IEEE Trans. Electromagn. Compat.*, vol. 49, no. 3, pp. 537–542, Aug. 2007.

[14] S. Wang, F. C. Lee, and W. G. Odendaal, "Cancellation of capacitor parasitic parameters for noise reduction application," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1125–1132, Jul. 2006.

[15] S. Wang, P. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.

[16] S. Wang, F. C. Lee, and W. G. Odendaal, "Single layer iron powder core inductor model and its effects on boost PFC EMI noise," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 15-–19, 2003, vol. 2, pp. 847–852.

[17] P. Kong, S. Wang, F. C. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1522–1533, May 2011.

[18] J. Biela and J. W. Kolar, "Using transformer parasitics for resonant converters—A review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008.

[19] F.-Y. Shih, Y.-T. Chen, Y.-P. Wu, and Y.-T. Chen, "A procedure for designing EMI filters for AC line applications," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 170–181, Jan. 1996.

[20] I. F. Kovacevic, T. Friedli, A. M. Muesing, and J. W. Kolar, "3-D electromagnetic modeling of EMI input filters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 231–242, Jan. 2014.

[21] S. Wang *et al.*, "Parasitic effects of grounding paths on common-mode EMI Filter's performance in power electronics systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3050–3059, Sep. 2010.

[22] S. Wang, F. C. Lee, and J. D. van Wyk, "Design of inductor winding capacitance cancellation for EMI suppression," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1825–1832, Nov. 2006.

[23] R. Kahoul, Y. Azzouz, B. Ravelo, and B. Mazari, "New behavioral modeling of EMI for DC motors applied to EMC characterization," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5482–5496, Dec. 2013.

[24] W. Wu *et al.*, "A new—filter with in-series parallel resonant circuit for single-phase grid-tied inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4640–4644, Sep. 2014.

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