A Current-Reference-Based Selective Harmonic Current Mitigation PWM Technique to Improve the Performance of Cascaded H-Bridge Multilevel Active Rectifiers

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***Abstract*—In this paper, a selective harmonic current mitigation pulsewidth modulation (SHCM-PWM) technique with low switching frequencies is proposed for grid-connected cascaded H-bridge multilevel rectifiers to fully meet harmonic requirements within extended harmonic spectrum. In the proposed technique, instead of using the voltage references to calculate switching angles for the rectifier as in conventional selective harmonic elimination-PWM (SHE-PWM) or selective harmonic mitigation-PWM (SHM-PWM), current references are used to compensate the current harmonics due to both grid voltage harmonics and rectifier input voltage harmonics so as to meet the current harmonic requirements and total demand distortion within the whole harmonic spectrum. Furthermore, the techniques to design the critical parameters including switching frequency, the highest harmonic order that can be mitigated using the proposed current-reference-based technique, and the coupling inductance that can attenuate the current harmonic orders above the highest order are investigated. With the same switching frequency, the proposed SHCM-PWM technique uses smaller coupling inductance to meet higher orders of current harmonic requirements than the conventional SHE-PWM technique. Finally, simulations and experiments were conducted to validate the proposed technique.**

***Index Terms*—Grid-tied multilevel rectifier, power quality, selective harmonic current mitigation pulsewidth modulation (SHCM-PWM), voltage harmonics.**

I. Introduction

THE cascaded H-bridge (CHB) topology plays an important role in high power electronics applications due to their low total harmonic distortion (THD), low electromagnetic interference, and high efficiency [1], [2]. Fig. 1 shows a grid tied, *i*-cell CHB ac/dc rectifier that has $2 \times i + 1$ output voltage levels [3]. The grid voltage is $V_{\mathrm{ac-Grid}}$. The input voltage of CHB is $V_{\mathrm{ac-CHB}}$, which is equal to the sum of the input voltages of all H-bridge cells. The current I_{in} flows from the power grid to CHB through two inductances, line inductance L_{grid}, and the inductance L_F of the coupling (filtering) inductor. The total inductance between the grid voltage source $V_{\mathrm{ac-Grid}}$ and the CHB rectifier is $L_T = L_{\mathrm{grid}} + L_F$. The dc-link voltages are equal to V_{dc}. The isolated dc/dc converters are connected to these dc links. The outputs of dc/dc converters are paralleled to charge energy storage on a dc bus. The loads, such as resistive load R_1 and electric vehicle (EV) charging load [3] in the figure, are connected to the dc bus through bidirectional dc/dc converters. The dc-link voltage, which has the second-order harmonic voltage ripple, of each H-bridge cell can be regulated either with the CHB dc-link voltage balancing strategy [3], [4], [13], [14] or via the isolated bidirectional dc/dc rectifiers in Fig. 1. Because voltage balancing and the reduction of the second-order harmonics on dc links are not the focus or contribution of this paper, they will not be discussed here. Because of this, in the analysis later, the dc link of each CHB cell is considered to be connected to a constant dc voltage sources V_{dc}. This does not void the validation of the principle of the proposed technique.

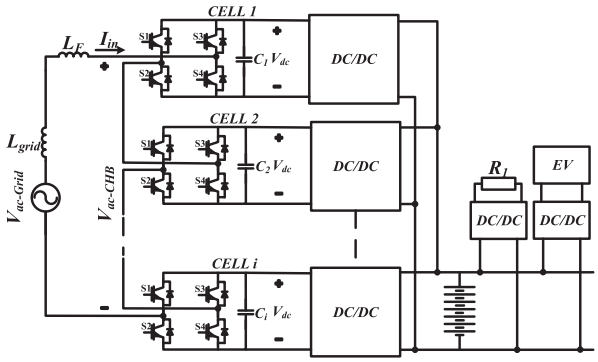

Fig. 1. Configuration of an *i*-cell, $(2i + 1)$-level single-phase grid-connected CHB converter.

The modulation techniques were developed for CHB-based power converters/inverters to meet not only the high efficiency requirements but also the power quality requirements [1], [2]. There are two existing optimal modulation techniques, selective

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harmonic elimination (SHE) technique [4]– [8] and selective harmonic mitigation (SHM) technique [9]– [11].

In [4] and [12], the transcendental equations were solved in the SHE-PWM approaches to reduce low-order harmonics. Although the techniques have high efficiency working at low switching frequencies, where the switching frequency is defined as the product of the number of switching transitions of each cell within one-quarter line period and the line frequency, the number of harmonics that can be eliminated is limited by the switching frequencies. For example, the maximum current harmonic order that can be eliminated is 25th when the switching frequency is three times of line frequency in a three-cell seven-level three-phase CHB power rectifier [4], [14]. However, in [13], in order to meet the current harmonic requirement, extra passive filters are needed. In addition, the influence of inductance L_F on the elimination or mitigation of current harmonics and the design technique for inductance L_F are not investigated in the literatures.

Optimal SHM-PWM is introduced in [9] for dc/ac multilevel inverters. The major advantage of the proposed technique is that it can mitigate higher order of harmonics than the conventional SHE-PWM with the same switching frequencies. This is because it just needs to reduce the harmonics to be lower than the standards instead of eliminating them [9]– [12]. Moreover, reducing the THD is also one of the targets of the SHM-PWM but not SHE-PWM. Finally, the conventional optimal SHM-PWM technique reduces current harmonics by reducing voltage harmonics of the CHB inverter so it cannot reduce the current harmonics due to grid voltage harmonics.

In [15], an unequal dc-link technique is used for SHM-PWM dc/ac cascaded inverters to reduce higher number of harmonics with minimized switching frequencies. However, the same issues in conventional SHM-PWM described in the last paragraph still exist.

In [16], a technique to obtain multiple SHE-PWM solutions is proposed. This technique can find the optimized solutions to eliminate harmonics up to 19th order with a three-cell inverter, however, it cannot meet the standard within full spectrum range and eliminate the current harmonics generated by grid voltage harmonics.

In [17], the SHE-PWM technique and conventional phase shift PWM (PSPWM) technique were compared in CHB inverter applications. It has been proved that the SHE-PWM technique can eliminate much higher number of harmonics than conventional PSPWM technique with the same number of switching frequencies. It is, therefore, reasonable to explore low-frequency modulation techniques such as SHE-PWM or SHM-PWM instead of the PSPWM technique for high power multilevel converters to improve energy efficiency.

In this paper, a selective harmonic current mitigation-PWM (SHCM-PWM) technique is proposed for grid-tied CHB multilevel ac/dc rectifiers (converters) to meet the harmonic standards such as IEEE-519 current distortion and total demand distortion (TDD) requirements. Compared with the existing SHM-PWM or SHE-PWM, the proposed technique has the following advantages.

1) The developed SHCM-PWM is directly applied to the currents $I_{\rm in}$ of grid-tied CHB ac/dc rectifiers; so the current harmonics due to grid voltage harmonics can be mitigated to below IEEE-519 current distortion limits, on the other hand, the existing SHM-PWM or SHE-PWM cannot reduce the current harmonics resulted from grid voltage harmonics.
2) The developed SHCM-PWM can mitigate higher orders of current harmonics based on the harmonic distortion percentage and TDD limits defined in IEEE-519 [18] than existing SHM-PWM or SHE-PWM with the same number of switching frequencies (transitions).
3) The influence of the coupling inductance L_F on the SHE-PWM, SHM-PWM, and SHCM-PWM in a CHB active rectifier is discussed and the coupling inductance design is investigated in this paper. It is shown that the proposed technique can meet both harmonic and TDD limits with smaller coupling inductance than SHE-PWM and SHM-PWM. The proposed technique can, therefore, reduce the cost and size of passive filters.

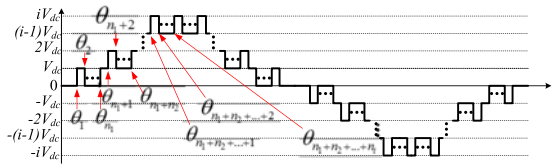

Fig. 2. Voltage waveform of a CHB active rectifier using the SHE-PWM, SHM-PWM, or SHCM-PWM techniques.

II. Proposed SCHM-PWM Technique for CHB Active Rectifiers

A. Conventional SHE-PWM in CHB Rectifiers

Both SHE-PWM and SHM-PWM techniques control switching angles to reduce low-order voltage harmonics of the CHB. SHE-PWM and SHM-PWM use Fourier series to obtain harmonic equations for $V_{\rm ac-CHB}$ [2]. In Fig. 1, the inductance L_T, which is equal to the sum of L_F and $L_{\rm grid}$ as defined in Section I, between the equivalent grid voltage source $V_{\rm ac-grid}$ and the CHB rectifier is designed to help reduce current harmonics. The voltages and currents on the ac side of the single-phase CHB active rectifier are

$$V_{\rm ac-Grid-}h = j\omega h L_T I_{\rm in-}h + V_{\rm ac-CHB-}h, \quad h = 1, 3, 5 \ldots \tag{1}$$

$$|I_{\rm in-}h| = \left| \frac{V_{\rm ac-Grid-}h - V_{\rm ac-CHB-}h}{\omega h L_T} \right| \tag{2}$$

where when $h = 1$, $V_{\rm ac-Grid-1}$, $V_{\rm ac-CHB-1}$ and $I_{\rm in-1}$ are the fundamental grid voltage, the fundamental input voltage and the fundamental input current of the CHB active rectifier respectively. When $h > 1$, $V_{\rm ac-Grid-}h$, $V_{\rm ac-CHB-}h$, and $I_{\rm in-}h$ are the grid voltage harmonics, input voltage harmonics, and input current harmonics, respectively. Equation (2) is the magnitude of the current harmonics flowing to the rectifier.

For the $V_{\rm ac-CHB}$ waveform in Fig. 2, the number of switching transitions in a quarter line period of the kth cell is n_k, $k = 1 \ldots i$. And the total number of switching transitions in a quarter line period is equal to $K = n_1 + n_2 + n_3 + \cdots + n_i$. Also, h

is the harmonic order and $\theta_1, \theta_2, \ldots, \theta_K$ are the switching angles.

In conventional SHE-PWM [4]– [8], [13], the grid voltage is considered to have zero harmonics, based on the Fourier theory and the $V_{\mathrm{ac-CHB}}$ waveform in Fig. 2, (1) can be rewritten as (3), shown at the bottom of the page, where $V_{\mathrm{ac-CHB}-h}$ is the hth voltage harmonic of the CHB active rectifier and it is determined by a_h and b_h. Because the waveform in Fig. 2 has quarter wave symmetry, the a_h and even order of b_h are equal to zero. The modulation index of $V_{\mathrm{ac-CHB}}$ is defined as

$$M_a = (\cos(\theta_1) - \cos(\theta_2) + \cdots + \cos(\theta_K)). \tag{4}$$

Furthermore, if $h \leq 2K-1$, all of the low-order harmonics $V_{\mathrm{ac-CHB}-3}$, $V_{\mathrm{ac-CHB}-5}$, $V_{\mathrm{ac-CHB}-7}, \ldots, V_{\mathrm{ac-CHB}-h}$ are equal to zero when SHE-PWM is applied. The equation for the voltage harmonics that can be eliminated in $V_{\mathrm{ac-CHB}-h}$ can be represented by

$$\begin{aligned} |V_{\mathrm{ac-CHB}-h}| = \frac{4V_{\mathrm{dc}}}{\pi h} &|\cos(h\theta_1) - \cos(h\theta_2) \\ &+ \cos(h\theta_3) + \cdots + \cos(h\theta_K)| = 0 \\ h &= 3, 5, \ldots 2K-1. \end{aligned} \tag{5}$$

The aforementioned equation shows the harmonics that can be eliminated in Fig. 2 with SHE-PWM. As shown in (5), the order of harmonics that can be eliminated by the SHE-PWM in a single-phase system is equal to $h = 2K-1$. As a result, with the SHE-PWM technique, when the grid has no voltage harmonics, the current harmonics in (3) can be written as

$$I_{\mathrm{in}-h} = \begin{cases} 0, & 3 \leq h \leq 2K-1 \\ -\frac{V_{\mathrm{ac-CHB}}}{j\omega h L_T}, & h > 2K-1. \end{cases} \tag{6}$$

In the aforementioned equation, because the objective of SHE-PWM is to eliminate $V_{\mathrm{ac-CHB}-h}$, it is defined as voltage reference modulation technique. There are following three issues for the conventional voltage reference SHE-PWM:

1) the effect of the grid voltage harmonics on $I_{\mathrm{in}-h}$ was not considered; but the current harmonics generated by grid voltage harmonics could be higher than current harmonic limits,
2) when $h > 2K-1$, the magnitudes of $I_{\mathrm{in}-h}$ can be higher than the current harmonic limits;
3) the inductance L_T design and its effect on harmonic elimination are not investigated.

B. SHM-PWM Technique for CHB Inverters

SHM-PWM technique proposed for CHB inverters [6], [9]–[11] uses voltage equation (7) to control switching angles. Instead of eliminating each harmonic, $V_{\mathrm{ac-CHB}-h}$ can be mitigated following

$$\begin{aligned} |V_{\mathrm{ac-CHB}-h}| = \frac{4V_{\mathrm{dc}}}{h\pi} &|\cos(h\theta_1) - \cos(h\theta_2) \\ &+ \cos(h\theta_3) + \cdots + \cos(h\theta_K)| \\ &\leq l_h \frac{4V_{\mathrm{dc}} M_a}{\pi}, h = 3, 5, \ldots. \end{aligned} \tag{7}$$

where l_h *is* the voltage harmonic limit, which is defined by the power quality standards. Moreover, the THD equation of $V_{\mathrm{ac-CHB}}$ can be controlled using (8), shown at the bottom of the page, by controlling the harmonic voltage $V_{\mathrm{ac-CHB}-h}$.

As discussed in [9], by reducing the voltage harmonics below the limits l_h instead of eliminating them, the SHM-PWM technique can reduce higher orders of harmonics than SHE-PWM with the same number of switching frequencies (transitions). Because of this, the SHM-PWM technique is more efficient than the SHE-PWM [10]. The issue of the SHM-PWM is that it does not guarantee always meeting current harmonic requirement as it takes voltage limit as its reference. It cannot reduce the current harmonics due to grid voltage harmonics. Furthermore, it does not consider the effect of L_T on $I_{\mathrm{in}-h}$. In this paper, the SHM-PWM technique is extended to rectifiers and a new SHCM-PWM is developed.

C. Proposed SHCM-PWM Technique for CHB Active Rectifiers

Although SHM-PWM can control more orders of voltage harmonics than the SHE-PWM technique, its objective is still to meet the voltage harmonic limits instead of current harmonic limits. At the same time, the current harmonics need meet harmonic limits for most applications such as grid-tied converters or inverters. In the proposed SHCM-PWM technique, instead of using the voltage limits to control $V_{\mathrm{ac-CHB}-h}$, the harmonic current limits are used in (2) to control CHB's current harmonics due to both the grid voltage and CHB voltage harmonics. The phasor diagram of (1) is shown in Fig. 3. The difference between the grid voltage harmonic $V_{\mathrm{ac-Grid}-h}$ and the CHB rectifier input voltage harmonic $V_{\mathrm{ac-CHB}-h}$ determines the voltage drop

$$\begin{cases} j\omega L_T I_{\mathrm{in}-h} + V_{\mathrm{ac-CHB}-h} = 0 \Rightarrow I_{\mathrm{in}-h} = \frac{-V_{\mathrm{ac-CHB}-h}}{j\omega h L_T}, & \text{for } h = 3, 5, \ldots \\ V_{\mathrm{ac-CHB}} = \sum_{h=1}^{\infty} \frac{4V_{\mathrm{dc}}}{\pi h}(a_h \cos(h\omega t) + b_h \sin(h\omega t)) \\ a_h = -\sin(h\theta_1) + \sin(h\theta_2) - \cdots - \sin(h\theta_K) \\ b_h = \cos(h\theta_1) - \cos(h\theta_2) + \cdots + \cos(h\theta_K) \end{cases} \tag{3}$$

$$\mathrm{THD} = \frac{\sqrt{|V_{\mathrm{ac-CHB}-3}|^2 + |V_{\mathrm{ac-CHB}-5}|^2 + |V_{\mathrm{ac-CHB}-7}|^2 + \cdots + |V_{\mathrm{ac-CHB}-\infty}|^2}}{\frac{4V_{\mathrm{dc}}}{\pi} M_a}. \tag{8}$$

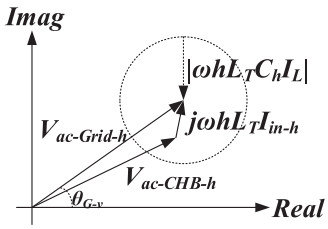

Fig. 3. Phasor diagram of (1).

$j\omega h L_T I_{\mathrm{in}-h}$ on the inductor. In order to analyze the worst scenario, the voltage harmonics of grid voltage $V_{\mathrm{ac}-\mathrm{Grid}-h}$ is equal to the maximum allowed voltage harmonic limit in IEEE-519. It is 3% of fundamental voltage. Significant voltage harmonics exist even at utility voltage level (120 V/220 V) as shown later in the experiments. Because all current harmonics generate voltage drops on inductor L_T, and all current harmonics need meet IEEE-519 current harmonic limit, the highest allowable voltage drop of the hth order current harmonic $I_{\mathrm{in}-h}$ on inductor L_T can be determined as $\omega h L_T C_h I_L$, where C_h is the current harmonic requirements of IEEE-519 and I_L is the maximum rectifier load current defined in the IEEE-519.

Because the phases of these voltage drops due to current harmonics can be any angle from 0 to 2π and the actual voltage drop of the hth order current harmonic $I_{\mathrm{in}-h}$ should be smaller than $\omega h L_T C_h I_L$ to meet the current harmonic limit, from Fig. 3, the range of the inductor voltage drop due to the harmonic current $I_{\mathrm{in}-h}$, which meets current harmonic limit is a circle with radius equal to $\omega h L_T C_h I_L$ and it centers the end of $V_{\mathrm{ac}-\mathrm{Grid}-h}$. If $V_{\mathrm{ac}-\mathrm{CHB}-h}$ is inside the circle, the difference $\omega h L_T I_{\mathrm{in}-h}$ between the grid voltage harmonic $V_{\mathrm{ac}-\mathrm{Grid}-h}$ and CHB voltage harmonic $V_{\mathrm{ac}-\mathrm{CHB}-h}$ meets the following condition:

$$|\omega h L_T I_{\mathrm{in}-h}| \le |\omega h L_T C_h I_L|. \tag{9}$$

In other words, with the hth order CHB voltage harmonic $V_{\mathrm{ac}-\mathrm{CHB}-h}$ and the hth order grid voltage harmonic $V_{\mathrm{ac}-\mathrm{Grid}-h}$, the current harmonic $I_{\mathrm{in}-h}$ can meet the current harmonic limit. In Fig. 3, C_h is determined by IEEE-519. The radius of the circle of each order harmonic depends only on the inductance L_T if the load current I_L of the CHB active rectifier and the grid voltage frequency ω are known. Two cases are to be analyzed in the following: small inductance case in Fig. 4(a) and (b) and big inductance case in Fig. 5(a) and (b).

1) Small Inductance L_T: Because the phase angles of $V_{\mathrm{ac}-\mathrm{Grid}-h}$ and $V_{\mathrm{ac}-\mathrm{CHB}-h}$ vary from 0 to 2π, Fig. 4(a) and (b) shows the phasor diagram of the grid voltage harmonics $V_{\mathrm{ac}-\mathrm{Grid}-h}$ and the voltage drop of the inductor $\omega h L_T I_{\mathrm{in}-h}$, when the inductance is small. To meet the current harmonic requirements, the CHB voltage must generate voltage vectors located inside the dash-line boundary circle. The boundary circle has a radius equal to $\omega h L_T C_h I_L$ and centers on another circle, which centers origin and has a radius determined by $V_{\mathrm{ac}-\mathrm{Grid}-h}$. In Fig. 4(b), to meet the limits, $V_{\mathrm{ac}-\mathrm{CHB}-h}$ must be solved for all possible phases of the grid voltage harmonics and the solutions will be stored in lookup table (LUT), so the LUT should have enough space to store all data.

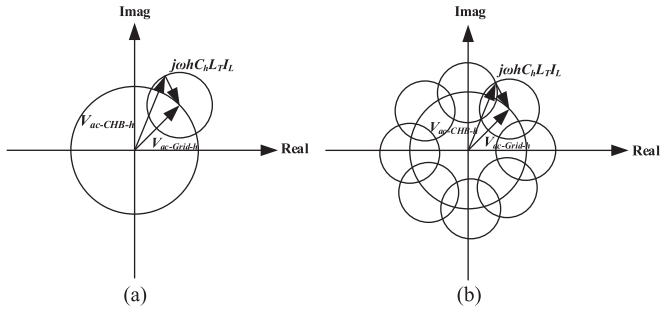

Fig. 4. Phasor diagram of the $V_{\mathrm{ac}-\mathrm{Grid}-h} + j\omega h L_T I_{\mathrm{in}-h}$ with small L_T and a harmonic limit circle, (a) for a specific case and (b) when grid voltage phases varies from 0 to 2π.

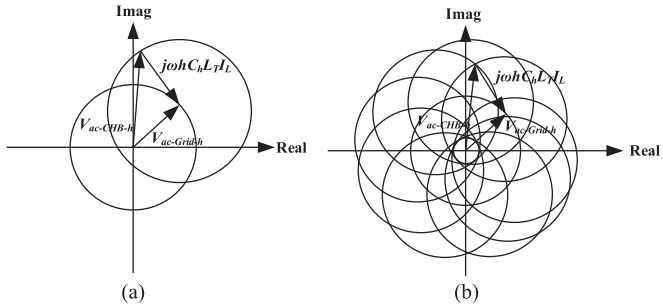

Fig. 5. Phasor diagram of the $V_{\mathrm{ac}-\mathrm{Grid}-h} + j\omega h L_T I_{\mathrm{in}-h}$ with big L_T, (a) for a specific case and (b) when grid voltage phases varies from 0 to 2π.

In (6), for the SHE-PWM, the CHB rectifier generates zero-voltage harmonics below the order of $2K-1$. So, the $V_{\mathrm{ac}-\mathrm{Grid}-h}$ contributes to $I_{\mathrm{in}-h}$ and $I_{\mathrm{in}-h}$ can be higher than the limit $C_h I_L$ defined in IEEE-519. The voltage drop of the $I_{\mathrm{in}-h}$ on the inductor is equal to $V_{\mathrm{ac}-\mathrm{Grid}-h}$. It can be higher than the $\omega h L_T C_h I_L$, which is the voltage drop of the harmonic current limit on the inductor. This can be described as

$$I_{\mathrm{in}-h} = \frac{|V_{\mathrm{ac}-\mathrm{Grid}-h}|}{|\omega h L_T|} \ge C_h I_L \tag{10}$$

$$|V_{\mathrm{ac}-\mathrm{Grid}-h}| = \omega h L_T I_{\mathrm{in}-h} \ge \omega h L_T C_h I_L. \tag{11}$$

If L_T is smaller than the critical inductance $L_{\mathrm{crt}-h}$ as shown in the following equation, the harmonics cannot meet the limits:

$$L_T \le L_{\mathrm{crt}-h} = \frac{|V_{\mathrm{ac}-\mathrm{Grid}-h}|}{\omega h C_h I_L}. \tag{12}$$

As shown in the aforementioned equation, if the inductance is smaller than $L_{\mathrm{crt}-h}$, it is impossible to meet IEEE-519 using SHE-PWM. Similarly, for the SHM-PWM and SHCM-PWM, if the inductance is smaller than $L_{\mathrm{crt}-h}$, because it is impossible to control the phase of the $V_{\mathrm{ac}-\mathrm{CHB}-h}$, the harmonics cannot meet the limits too.

2) Big Inductance L_T: As shown in Fig. 5(a), if L_T is bigger than the critical inductance $L_{\mathrm{crt}-h}$ as shown in the following equation, the circle of the voltage drop $\omega h L_T C_h I_L$ contains the

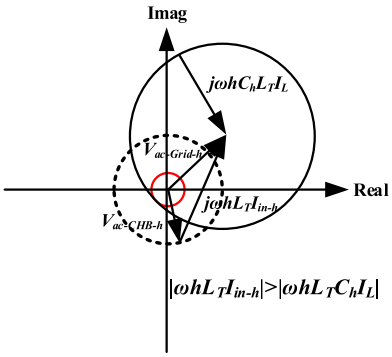

Fig. 6. Phasor diagram of $V_{\mathrm{ac-Grid}-h} + j\omega h L_T I_{\mathrm{in}-h}$ when the SHM-PWM technique is used with big L_T.

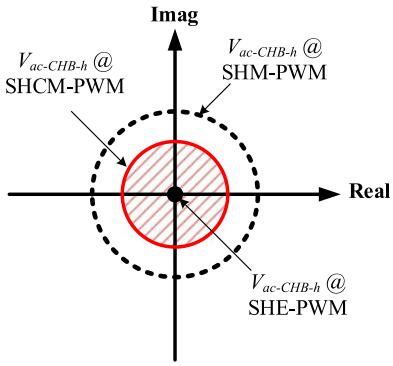

Fig. 7. Comparison of SHE-PWM, SHM-PWM, and SHCM-PWM to generate $V_{\mathrm{ac-CHB}-h}$ in order to meet current harmonic limits with a big L_T.

origin of the plane:

$$L_T \geq \frac{|V_{\mathrm{ac-Grid}-h}|}{\omega h C_h I_L} = L_{\mathrm{crt}-h}. \tag{13}$$

Because of this, as shown in Fig. 5(b), when grid voltage phases vary from 0 to 2π, there is a small circle centering the origin. If this circle is called safe circle, inside the safe circle, $V_{\mathrm{ac-CHB}-h}$ does not need to consider the phase to meet the current harmonic limits. The radius r_h of the safe circle is

$$r_h = |\omega h L_T C_h I_L| - |V_{\mathrm{ac-Grid}-h}|. \tag{14}$$

Based on the aforementioned analysis, for SHE-PWM with inductance L_T higher than $L_{\mathrm{crt}-h}$, the $V_{\mathrm{ac-CHB}-h}$ is zero so it is always within the safe circle when the harmonic order is smaller than $2K-1$. For the harmonic orders higher than $2K-1$, the CHB voltage harmonics cannot be eliminated and so the current harmonics can exceed the limits. Also, the $V_{\mathrm{ac-CHB}-h}$ for the SHM-PWM, when the voltage harmonic requirements (such as voltage distortion requirements in IEEE 519 [18]) are met based on (7), can be illustrated by the dashed circle region in Fig. 6. Because the radius of the dash circle depends on the harmonic standard, it can be higher than r_h in (14). As a result, the SHM-PWM technique may not meet the standard even for low-order harmonics. Because of this, SHE-PWM is better than SHM-PWM when grid voltage harmonics are present. On the other hand, the current-reference-based SHCM-PWM can generate $V_{\mathrm{ac-CHB}}$ inside the small red safe circle when grid voltage harmonics are present in Fig. 6. Because at high-order harmonics, the optimization range is increased [8]– [11] for the mitigation technique, the number of CHB voltage harmonics that can be mitigated to be within the safe circle is much higher than that with SHE-PWM and SHM-PWM. Consequently, although when L_T is smaller than $L_{\mathrm{crt}-h}$, none of SHE-PWM, SHM-PWM, and SHCM-PWM can reduce the current harmonics resulted from the grid voltage harmonics, whose magnitudes equal to the limits of IEEE 519, to below the current limits, SHCM-PWM can mitigate higher order of harmonics to below the limits than SHE-PWM and SHM-PWM when L_T is bigger than $L_{\mathrm{crt}-h}$. Fig. 7 also shows the comparison between SHE-PWM, SHM-PWM, and SHCM-PWM techniques to generate $V_{\mathrm{ac-CHB}-h}$. As discussed before, to meet the requirement of IEEE 519 for the hth order harmonic without controlling the phases of CHB voltage (when $L_T \geq L_{\mathrm{crt}-h}$), the $V_{\mathrm{ac-CHB}-h}$ must be inside the red safe circle in Fig. 7. For the SHE-PWM technique, to eliminate low-order harmonics, the $V_{\mathrm{ac-CHB}-h}$, the black dot at the origin of the plane in Fig. 7, is close to the origin of the plane. As a result, the low-order harmonics can meet the current harmonic limits; however, the noneliminated high-order harmonics can be outside of the safe circle. For the SHM-PWM technique, the voltage harmonic limits instead of current harmonic limits are used. These voltage harmonic limits (dashed circle) can be bigger than safe circle (shaded circle), as shown in Fig. 7. Hence, even for low-order harmonics, the SHM-PWM may not meet the current harmonic limits. On the other hand, for the proposed SHCM-PWM technique, the $V_{\mathrm{ac-CHB}-h}$ is always inside the safe circle. So, the $I_{\mathrm{in}-h}$ can always meet the current harmonic limits.

TABLE I
CIRCUIT PARAMETERS OF THE GRID-CONNECTED CHB RECTIFIER

Parameter	Symbol	Value
Line frequency	f	60 Hz
AC grid Voltage (RMS)	V_{ac}	110 V
Rectifier total power	P_{total}	1.5 kW
Maximum Demand Load (RMS)	I_L	14.14 A

3) Simulation Verification: Simulations were conducted to validate the analysis. In the simulations, the magnitudes of the grid harmonic voltages are the same as the voltage limit of IEEE-519 (the worst scenario) and the phases of grid voltage harmonics change from 0 to 2π. The third-order harmonic will be investigated as an example. The verification can be applied to other orders of harmonics. The circuit parameters of the CHB active rectifier used in the simulations are in Table I.

In Figs. 4(a) and 5(a), within the boundary circle

$$V_{\mathrm{ac-CHB}-h} = |V_{\mathrm{ac-Grid}-h}|\angle\theta_{\mathrm{Gv}-h} - |\omega h L_T I_{\mathrm{in}-h}|\angle(\theta_{i\mathrm{CHB}-h} + 90^\circ) \tag{15}$$

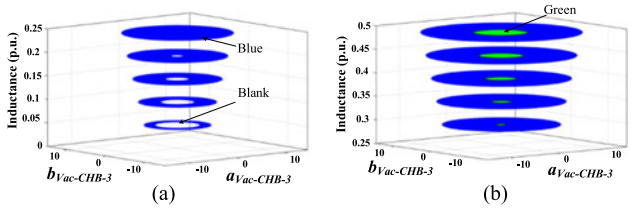

Fig. 8. Solutions $a_{V_{\mathrm{ac-CHB-3}}}$ and $b_{V_{\mathrm{ac-CHB-3}}}$ of the third-order CHB voltage $V_{\mathrm{ac-CHB-3}}$ in (16): (a) for the inductance from 0.0485 to 0.25 p.u. and (b) for the inductance from 0.25 to 0.485 p.u.

where $I_{\mathrm{in}-h} < C_h I_L$; the θ_{Gv-h} and $\theta_{i\mathrm{CHB}-h}$ are the phases of the grid harmonic voltage $V_{\mathrm{ac-Grid}-h}$ and harmonic current $I_{\mathrm{in}-h}$, respectively. The real component $a_{V_{\mathrm{ac-CHB}-h}}$ and imaginary component $b_{V_{\mathrm{ac-CHB}-h}}$ of the hth CHB voltage harmonic within the boundary circle in (15) can be written as

$$\begin{aligned} a_{V_{\mathrm{ac-CHB}-h}} &= |V_{\mathrm{ac-Grid}-h}|\cos(\theta_{\mathrm{Gv}-h}) \\ &\quad - |\omega h L_T I_{\mathrm{in}-h}|\cos(\theta_{i\mathrm{CHB}-h} + 90^\circ) \\ b_{V_{\mathrm{ac-CHB}-h}} &= |V_{\mathrm{ac-Grid}-h}|\sin(\theta_{\mathrm{Gv}-h}) \\ &\quad - |\omega h L_T I_{\mathrm{in}-h}|\sin(\theta_{i\mathrm{CHB}-h} + 90^\circ). \end{aligned} \quad (16)$$

By sweeping $I_{\mathrm{in}-h}$ from 0 to $C_h I_L$, sweeping L_T from 1 mH (0.0485 p.u.) to 10 mH (0.485 p.u.), sweeping θ_{Gv-h} from 0 to 2π and sweeping $\theta_{i\mathrm{CHB}-h}$ from 0 to 2π in (16), the results of $a_{V_{\mathrm{ac-CHB-3}}}$ and $b_{V_{\mathrm{ac-CHB-3}}}$ for the third-order harmonic are shown as both blue and green regions in Fig. 8. If the r_h defined in (14) is larger than zero, for any $V_{\mathrm{ac-CHB}-h} = a_{V_{\mathrm{ac-CHB}-h}} + j b_{V_{\mathrm{ac-CHB}-h}}$, which can meet the condition (17), it can meet the current harmonic limit disregard of its phase. The green safe circle regions on Fig. 7(b) represent these solutions.

$$\begin{aligned} \sqrt{|a_{V_{\mathrm{ac-CHB}-h}}|^2 + |b_{V_{\mathrm{ac-CHB}-h}}|^2} &\le r_h \\ &= |\omega h L_T C_h I_L| - |V_{\mathrm{ac-Grid}-h}|. \end{aligned} \quad (17)$$

As shown in Figs. 4(a) and 8(a), when the inductance is small (between 0.04896 and 0.2448 p.u.), the CHB must control both the magnitude and phase of $V_{\mathrm{ac-CHB}-h}$ so it can be located in the blue rings to meet the current harmonic limits defined in IEEE-519. As discussed previously, with small inductance, because the SHE-PWM can only generate zero-voltage harmonics, the voltage $V_{\mathrm{ac-CHB}-h}$ is at the origin inside the blank circle region in Fig. 8(a). As a result, with small inductance, SHE-PWM cannot meet the limits of IEEE-519. Since SHM-PWM and SHCM-PWM do not control the phase of $V_{\mathrm{ac-CHB}-h}$, they cannot control $V_{\mathrm{ac-CHB}-h}$ to meet the limits too. In Fig. 8(b), both the blue ring and green safe circle regions are solutions to meet IEEE-519. As discussed previously in Fig. 5(b), the green safe circle region at the origin of the coordinate is the region that $V_{\mathrm{ac-CHB}-h}$ can meet the limit disregard its phase. By using enough inductance L_T in Fig. 5(b) or 8(b), r_h will be larger than zero. Harmonic limits can be met as long as condition (17) is met. Higher number of harmonics can be mitigated with the SHCM-PWM than with SHM-PWM or SHE-PWM as discussed previously.

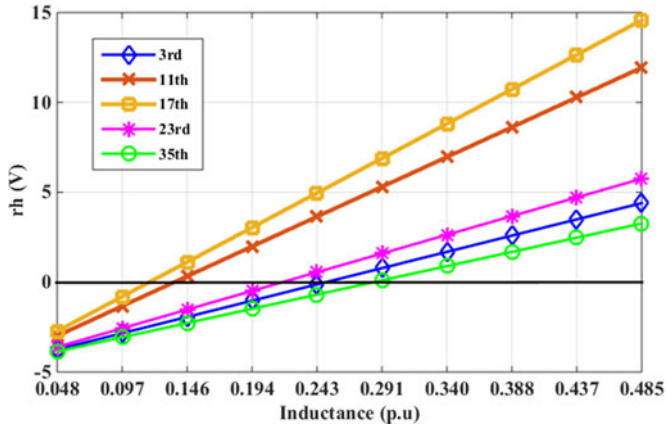

Fig. 9. r_h as a function of L_T and harmonic orders 3rd, 11th, 17th, 23rd, and 35th.

III. Inductance and Switching Frequency Design for SHCM-PWM

As discussed in Section II, inductance L_T should be big enough to achieve high-order harmonic compensation. For the inductance design in SHE-PWM, SHM-PWM, and SHCM-PWM, two requirements must be considered; First, the inductance must be big enough to keep $r_h > 0$ so that SHE-PWM, SHM-PWM, and SHCM-PWM can meet the low-order harmonic limits. In the green safe circle region in Fig. 8(b), without increasing the switching frequency of the rectifier, SHCM-PWM can meet higher order harmonic limits without controlling the phase than SHE-PWM and SHM-PWM [19]. Second, the inductance must be big enough to attenuate the high-order current harmonics, which cannot be eliminated or mitigated with SHE-PWM, SHM-PWM, and SHCM-PWM to meet the limits. Two inductance design based on the two aforementioned requirements will be explored and the inductance design technique for the proposed SHCM-PWM will be developed.

A. Inductance Design Based on First Requirement

As discussed previously, IEEE 519 defines the C_h for different current harmonic orders, for a given L_T, the radius r_h of solid red safe circle in Fig. 6 and green safe circle regions in Fig. 8(b) can be calculated using (14). Because for the system under investigation, the ratio of the short-circuit current to the maximum load current is below 20, based on IEEE-519, C_h is 4% from 3rd to 9th, 2% from 11th to 15th, 1.5% from 17th to 21st, 0.6% from 23rd to 33rd and 0.3% above 35th-order harmonics. Based on (14), if $V_{\mathrm{ac-Grid}-h}$ is a constant equal to the voltage harmonic limit defined in IEEE-519, the r_h as a function of inductance L_T and harmonic order h can be drawn in Fig. 9. In Fig. 9, the inductance is from 1 (0.0485 p.u.) to 10 mH (0.485 p.u.). The curves of 3rd-, 11th-, 17th-, 23rd-, and 35th-order harmonics are investigated in Fig. 8 because they are the lowest harmonic orders of each C_h and based on (14) they have the smallest r_h for each C_h as $V_{\mathrm{ac-Grid}-h}$ is constant.

In Fig. 9, the r_h of the 35th-order harmonic has the strictest requirements as it is the smallest of all harmonics with the same L_T. Because r_h has to be larger than zero, the smallest

inductance that should be used for SHCM-PWM can be calculated as

$$|35\omega L_T C_{35} I_L| - |V_{\mathrm{ac-Grid-35}}| \geq 0 \tag{18}$$

$$L_T \geq \frac{|V_{\mathrm{ac-Grid-35}}|}{|35\omega C_{35} I_L|}. \tag{19}$$

From (19) and Fig. 9, the smallest inductance that must be used for the proposed SHCM-PWM is 5.8 mH or 0.281 p.u. It should be pointed out that the power line inductance is around 0.0485 p.u., which is much smaller than 0.281 p.u. Because of this, in this paper, it is assumed that $L_F \approx L_T$.

B. Inductance Design Based on Second Requirement

The inductance must also be designed to attenuate the high-order harmonics that are not mitigated using the SHE-PWM, SHM-PWM, and SHCM-PWM. From (3), because $b_h = 0$, the output voltage harmonics of the CHB rectifier can be written as

$$|V_{\mathrm{ac-CHB-}h}| = \frac{4V_{\mathrm{dc}}}{\pi h} |\cos(h\theta_1) - \cos(h\theta_2) + \cdots + \cos(h\theta_K)|. \tag{20}$$

Because Cos $|x| \leq 1$, $V_{\mathrm{ac-CHB-h}}$ meets the condition in

$$|V_{\mathrm{ac-CHB-}h}| = \frac{4V_{\mathrm{dc}}}{\pi h} |\cos(h\theta_1) - \cos(h\theta_2) + \cdots + \cos(h\theta_K)| \leq \frac{4V_{\mathrm{dc}}K}{\pi h}. \tag{21}$$

In Fig. 6, when $V_{\mathrm{ac-CHB-}h}$ reaches the maximum and is out of phase of $V_{\mathrm{ac-Grid-}h}$, the harmonic currents have the maximum voltage drops on the inductor. Under such condition, the harmonic current $I_{\mathrm{in-}h}$ should still meet the current harmonic limit $C_h I_L$. This is represented by (22). The minimum inductance L_T', which can always meet current harmonic limits for any high-order harmonics that are not mitigated using SHE-PWM, SHM-PWM, and SHCM-PWM, can therefore be derived from (23)

$$\frac{|V_{\mathrm{ac-CHB-}h}|_{\max} + |V_{\mathrm{ac-Grid-}h}|}{\omega h L_T{}'} = |I_{\mathrm{in-}h}|_{\max} \leq C_h I_L \tag{22}$$

$$L_T{}' \geq \frac{|V_{\mathrm{ac-CHB-}h}|_{\max} + |V_{\mathrm{ac-Grid-}h}|}{\omega h C_h I_L} = \frac{4V_{\mathrm{dc}}K}{\omega h^2 C_h I_L \pi} + \frac{|V_{\mathrm{ac-Grid-}h}|}{\omega h C_h I_L}. \tag{23}$$

In (23), L_T' decreases when h increases. Based on (23), because SHCM-PWM can mitigate higher orders of harmonics than SHE-PWM and SHM-PWM, L_T' in (23) can be significantly reduced. Because the output fundamental voltage of the CHB with SHCM-PWM must be higher than the grid voltage to achieve compensations, based on (3), the dc-link voltage of each CHB cell can be designed based on

$$\frac{4V_{\mathrm{dc}} \times i}{\pi} > \mathrm{Max}(V_{\mathrm{ac-Grid-1}}). \tag{24}$$

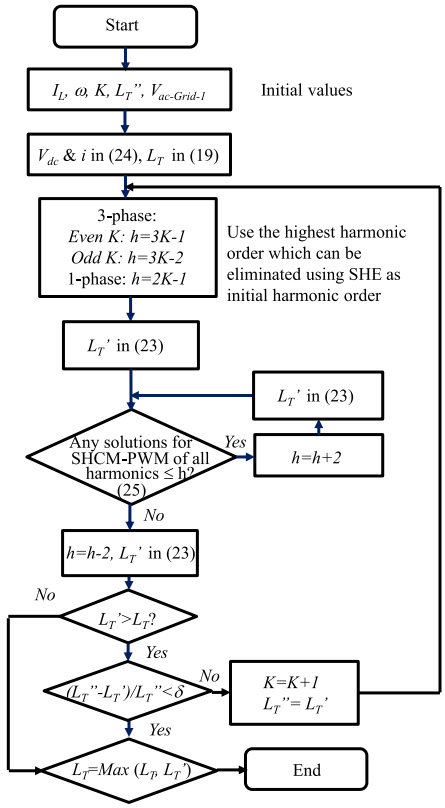

Fig. 10. Flowchart of designing parameters for the proposed SHCM-PWM.

C. Inductance Design for the Harmonic Reduction in Whole Spectrum

Because both low- and high-order current harmonics of the CHB active rectifier should meet the limits, the desired inductance L_T should be larger than the bigger one of (19) and (23). In addition, the inductance design should also meet TDD limit. Because of this, the objective function set (25) including the equation for modulation index M_a, inequations to meet current harmonic limits and to meet the TDD limit in IEEE 519 is used to find switching angle solutions $\theta_1 \ldots .\theta_k$ in SHCM-PWM for all harmonics below h

$$\begin{cases} M_a = \cos\theta_1 - \cos\theta_2 + \cos\theta_3 \cdots + \cos\theta_k \\ \sqrt{\left(\frac{I_{\mathrm{in-3}}}{I_L}\right)^2 + \left(\frac{I_{\mathrm{in-5}}}{I_L}\right)^2 + \cdots + \left(\frac{I_{\mathrm{in-}h}}{I_L}\right)^2 + \cdots} \leq C_{\mathrm{TDD}} \\ \frac{|V_{\mathrm{ac-Grid-}h}| + |V_{\mathrm{ac-CHB-}h}|}{|\omega h L_T I_L|} \leq C_h, \ h = 3, 5, 7, \ldots. \end{cases} \tag{25}$$

Fig. 10 shows the flowchart used to find the switching transition K that leads to the smallest inductance L_T and the highest harmonic order that can be mitigated with this inductance. In Fig. 10, initial values for the maximum load current I_L, grid frequency ω, switching transitions K, initial inductance L_T'' and grid voltage $V_{\mathrm{ac-Grid-1}}$ are first assigned. L_T'' is a big inductance to start with. DC-link voltage V_{dc} and the number i of cells are determined from (24). L_T is determined from (19). Because SHCM-PWM can mitigate higher order of harmonics

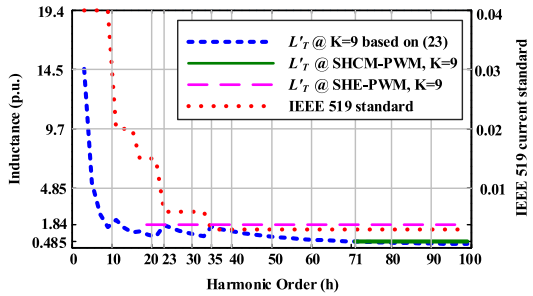

Fig. 11. Required inductance to meet high-order harmonics that cannot be reduced by modulation techniques.

than SHE-PWM and SHM-PWM, the highest order harmonics that can be eliminated with SHE-PWM is assigned as the initial h. The initial L'_T, which is needed to meet the second requirement, is calculated from (23). With the given K, h will continuously increase and L'_T will be updated (reduced) based on new h as long as SHCM-PWM has solutions for all harmonics below h. The highest h obtained will be used to calculate the final L'_T of this iteration using (23) for the given K. The L'_T will be compared with the L_T determined by (19). If L'_T is smaller than L_T, the final L_T will be the L_T determined by (19). Otherwise, L'_T will be compared with L''_T, which is the L'_T in the last iteration. If the ratio of the difference between L''_T and L'_T to L''_T is bigger than a predefined threshold δ (for example, 5%), K will be increased for another iteration to get smaller L'_T and solutions for (25) until L'_T is close to the minimum value (δ determines how close it is) or smaller than the L_T determined by (19). The bigger one of L_T and L'_T will be selected as the final L_T. By following Fig. 10, K and L_T can meet the requirements of (19), (23), and (25). The switching transitions K (switching frequency $= K\omega/(2i\pi)$) and the smallest L_T are designed. The highest harmonic order h, which can be mitigated with SHCM-PWM to be below the limit, is identified. With this K and L_T, SHCM-PWM can mitigate the harmonics to be below the limits up to order h. L_T can attenuate the harmonics higher than h to be below the limits. Furthermore, harmonics can meet TDD limit. To solve (25) in Fig. 9, a multiobjective particle swarm optimization technique [20] is used in this paper. Following the flowchart, parameters came out as $K = 9$; $h = 69$th, $i = 3$, $L_F = 10$ mH (0.485 p.u.) for the specs given in Table I.

In order to compare the proposed SHCM-PWM using the SHE-PWM and SHM-PWM techniques with the same number of switching transitions for both single-phase and three-phase CHB active rectifiers, the required inductance $L_T \approx L_F$ that can meet the high-order harmonic requirement in (23) is shown in Fig. 11 from 3rd to 100th harmonic orders. With the SHE-PWM technique, when $K = 9$, the highest harmonic order that can be eliminated is 17th in the single-phase and 25th in three-phase systems. As shown in Fig. 11, in order to guarantee that all of the harmonics higher than 17th for single-phase or 25th for three-phase systems can meet IEEE-519, the smallest inductance that should be used with SHE-PWM is 38 mH (1.84 p.u.) in single-phase or 34 mH (1.65 p.u) in three-phase systems. In the single-phase CHB with an SHM-PWM technique, the

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS FOR A GRID-CONNECTED CHB RECTIFIER

Parameter	Symbol	Value
Number of H-bridge cells	i	3
DC bus voltage	$V_{\rm dc}$	70 V
Input inductance	L_F	10 mH (0.485 p.u.)

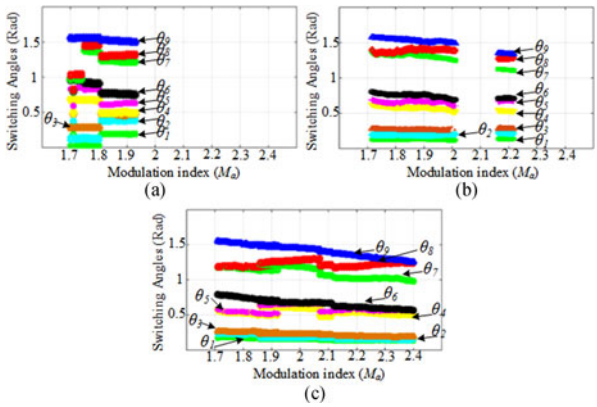

Fig. 12. Solutions of the optimization techniques: (a) SHE-PWM technique, (b) SHM-PWM technique, and (c) SHCM-PWM technique.

TABLE III
COMPARISON OF MODULATION TECHNIQUES

Modulation Technique	Switching Frequency	Number of Harmonics That can be Controlled	Required Inductance (p.u.) to Meet Current Harmonic Limits
SHE-PWM	180 Hz	17th	1.16 p.u. (24 mH)
SHM-PWM	180 Hz	23rd	0.728 p.u. (15 mH)
SHCM-PWM	180 Hz	69th	0.485 p.u. (10 mH)

highest harmonics that can be mitigated to meet the requirements of IEEE 519 with $K = 9$ is 23rd. A 34-mH (1.65 p.u.) inductance should be used for single-phase SHM-PWM technique. On the other hand, the SHCM-PWM can meet IEEE-519 up to 69th order (it will be shown later), the smallest inductance that can meet IEEE-519 for high-order harmonics in both single- and three-phase systems is around 10 mH (0.485 p.u.) with $K = 9$. The circuit parameters, which are used in both simulations and experiments, are shown in Table II. Other parameters are given by Table I.

The final switching angle solutions are obtained by following the flowchart in Fig. 10 and shown in Fig. 12(c). The switching angle solutions for SHE-PWM and SHM-PWM are shown in Fig. 12(a) and (b). Because many papers have discussed the technique to find the solutions for SHE-PWM and SHM-PWM, it will not be discussed here. As shown in this figure, the solution ranges of SHE-PWM and SHM-PWM techniques are much lower than the proposed SHCM-PWM technique. The comparison of the required inductance to meet both harmonic and TDD limits for SHE-PWM, SHM-PWM, and the proposed SHCM-PWM is shown in Table III. As shown, with the same switching

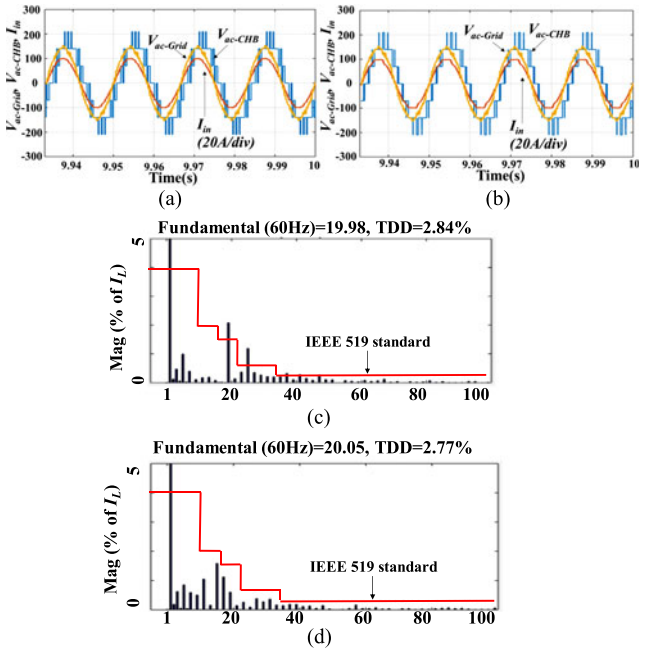

Fig. 13. Simulation results of conventional SHE-PWM and the SHCM-PWM with $M_a = 1.93$, (a) time-domain waveforms when SHE-PWM is applied, (b) time-domain waveforms when SHCM-PWM is applied, (c) current harmonic distortion of SHE-PWM, and (d) current harmonic distortion of SHCM-PWM.

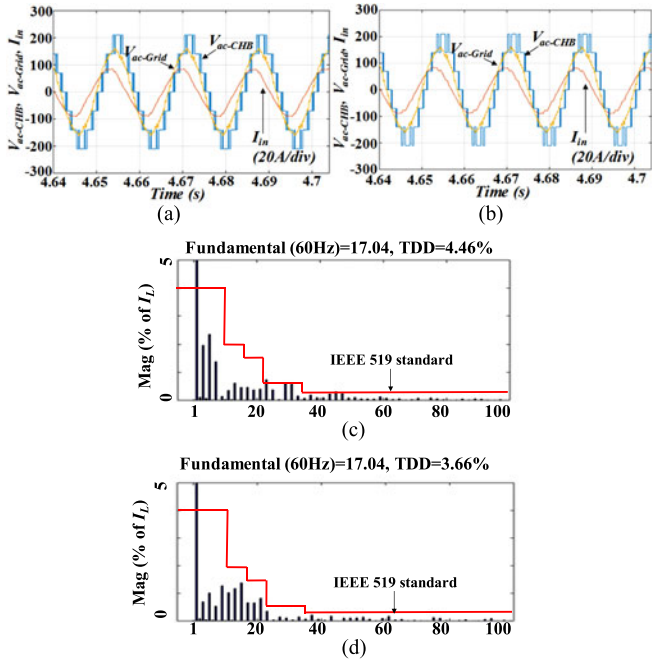

Fig. 14. Simulation results of SHM-PWM and the SHCM-PWM with $M_a = 2.16$, (a) time-domain waveforms when SHM-PWM is applied, (b) time-domain waveforms when SHCM-PWM is applied, (c) current harmonic distortion of SHM-PWM, and (d) current harmonic distortion of SHCM-PWM.

frequency 180 Hz for each cell, the proposed SHCM-PWM technique needs the smallest inductance.

IV. Simulation and Experimental Validation

A. Simulation Verification

The simulation verification was made in MATLAB Simulink. The simulation circuit is the same as Fig. 1 with $i = 3$, $k = 9$, and $n_1 = n_2 = n_3 = 3$. The dc/dc rectifiers were replaced with voltage source $V_{\rm dc}$ as explained before. The circuit parameters are the same as in Tables I and II. The proposed SHCM-PWM and the SHE-PWM and SHM-PWM were simulated. Two operating points were simulated: $M_a = 1.93$ with unity power factor and $M_a = 2.16$ with 0.89 leading power factor. Fig. 13(a) and (b) shows the simulated $V_{\rm ac-Grid}$, $V_{\rm ac-CHB}$, and $I_{\rm in}$ when the modulation index is equal to 1.93 with SHE-PWM and the proposed SHCM-PWM, respectively. The grid voltage has voltage distortions as shown in Fig. 13(a) and (b). Fig. 13(c) and (d) are the simulated harmonic distortions with conventional SHE-PWM and with the proposed SHCM-PWM, respectively. It is shown in Fig. 13(c) and (d) that, because the switching angles are optimized for all of the harmonics up to 69th order, the proposed SHCM-PWM can meet both current harmonic and TDD limits of IEEE-519. On the other hand, based on the analysis in Section II-A, SHE-PWM can only eliminate harmonics up to 17th, so although SHE-PWM meet TDD limit, the 19th, 25th, 37th, 41st, and 47th harmonics do not meet limits. Fig. 14(a) and (b) shows the simulated $V_{\rm ac-Grid}$, $V_{\rm ac-CHB}$, and $I_{\rm in}$ with $M_a = 2.16$ and 0.89 leading power factor for SHM-PWM and SHCM-PWM, respectively. Fig. 14(c) and (d) shows the simulated harmonic distortion with SHM-PWM and the SHCM-PWM, respectively. For SHM-PWM, the 23rd, 29th, 31st, 43rd, and 45th harmonics do not meet IEEE-519. On the other hand, the SHCM-PWM can meet up to 100th-order harmonic limits. The TDD is 3.66%, which meets 5% TDD limit too. It should be noted that grid harmonics are also extracted and included in the simulations. To simulate grid voltage distortions, a grid voltage waveform is first measured with an oscilloscope and its harmonic spectrum is extracted using FFT up to 40th order, which is usually considered as the upper limit for THD calculation in literatures. The extracted grid voltage harmonics, which include both magnitudes and phases, are added to an ideal grid voltage in the simulations.

B. Experimental Verification

The SHCM-PWM technique can be applied to any grid voltage levels. A CHB prototype, which has the same circuit as used in the simulations and the same parameters as in Tables I and II, is tied to a utility grid with an open-loop control to validate the proposed modulation technique as shown in Fig. 15. TMS320F28335 digital signal controller was used in experiments. The actual utility grid has significant voltage harmonics as shown in Fig. 16(a). As shown in the function block in Fig. 16(b), open-loop control is used in prototype for demonstration purpose. The input parameters $\Delta\theta_{R-G}$, which is the phase between the fundamental of CHB voltage and grid voltage, and M_a, which is the modulation index as defined previously, are used to achieve desired power control. Fig. 17(a) and (b) shows the measured time-domain waveforms with 1.93 modulation

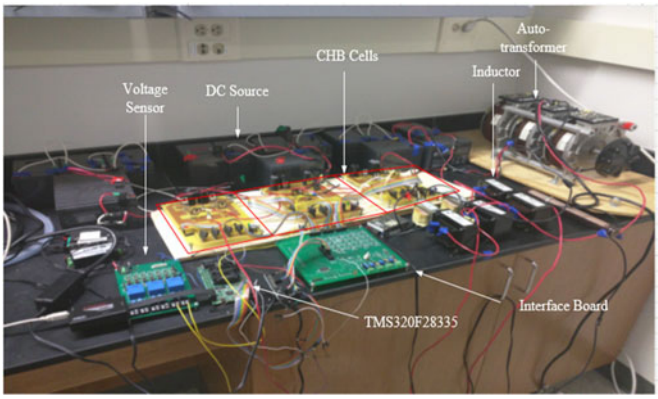

Fig. 15. Hardware prototype of the grid-tied seven-level CHB converter.

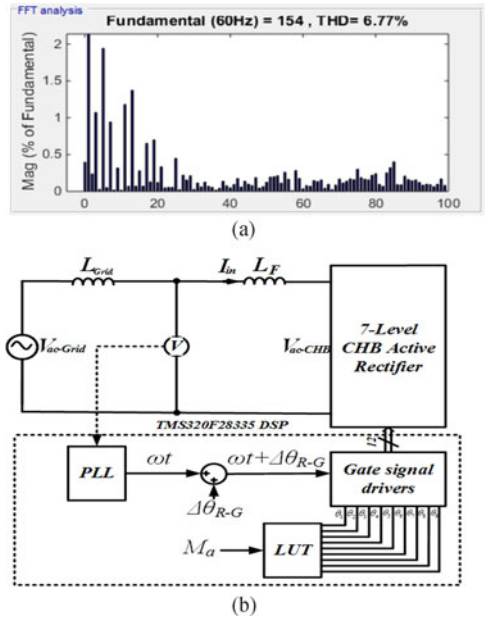

Fig. 16. (a) Actual grid voltage harmonics, (b) function block of hardware.

index and unity power factor using SHE-PWM and SHCM-PWM, respectively. Fig. 17(c) shows the measured harmonics for $I_{\rm in}$ with SHE-PWM. For the same reason as simulations, SHE-PWM can only eliminate harmonics up to 17th. The 19th, 25th, and 41st harmonics are higher than the limits. The measured TDD is 3.58%. On the other hand, in Fig. 17(d), the current harmonics of SHCM-PWM can meet the limits up to 100th order and its 3.53% TDD is smaller than 5% TDD limit.

Fig. 18(a) and (b) shows the $V_{\rm ac-Grid}$, $V_{\rm ac-CHB}$, and $I_{\rm in}$ with $M_a = 2.16$ and 0.89 leading power factor for SHM-PWM and SHCM-PWM, respectively. Fig. 18(c) shows the current harmonic waveform of the SHM-PWM. It is obvious that the 3rd-, 23rd-, 31st-, and 43rd-order current harmonics cannot meet the limits. Its 5.64% TDD cannot meet the 5% TDD limit too. On the other hand, the current harmonics caused by the voltage harmonics of $V_{\rm ac-Grid}$ can still be reduced with the proposed SHCM-PWM in Fig. 18(d). It is shown that all current harmonic distortions are within the IEEE-519 limits. The measured TDD is 4.1%, which also meets the 5% limit.

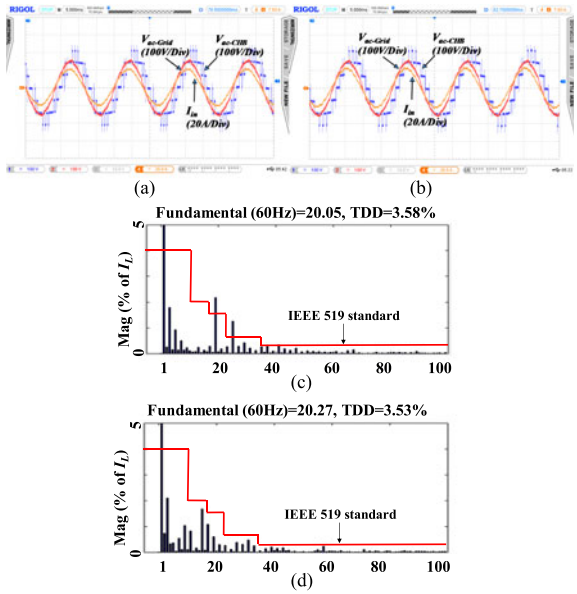

Fig. 17. Experimental results for SHE-PWM and SHCM-PWM on a grid-tied CHB rectifier when $M_a = 1.93$: (a) $V_{\rm ac-Grid}$, $V_{\rm ac-CHB}$ and $I_{\rm in}$ with SHE-PWM, (b) $V_{\rm ac-Grid}$, $V_{\rm ac-CHB}$, and $I_{\rm in}$ with SHCM-PWM, (c) harmonic spectrum of $I_{\rm in}$ with SHE-PWM, and (d) harmonic spectrum of $I_{\rm in}$ with SHCM-PWM.

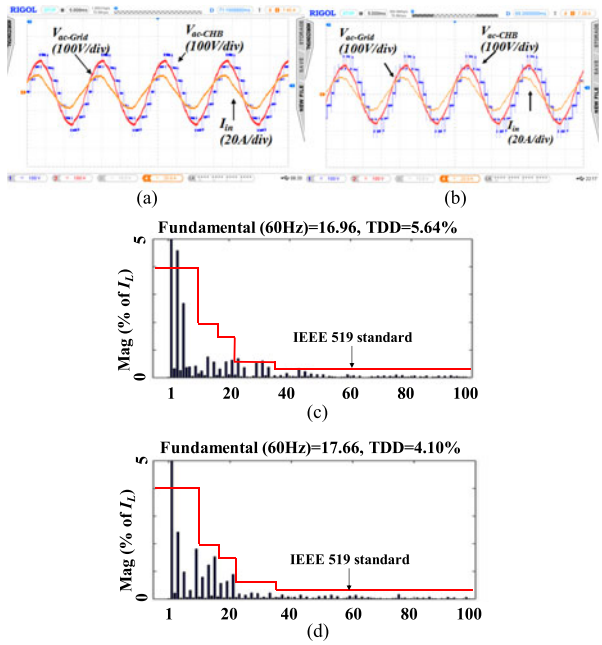

Fig. 18. Experimental results for SHM-PWM and SHCM-PWM on a grid-tied CHB rectifier when $M_a = 2.16$: (a) $V_{\rm ac-Grid}$, $V_{\rm ac-CHB}$ and $I_{\rm in}$ with SHM-PWM, (b) $V_{\rm ac-Grid}$, $V_{\rm ac-CHB}$, and $I_{\rm in}$ with SHCM-PWM, (c) harmonic spectrum of $I_{\rm in}$ with SHM-PWM, and (d) harmonic spectrum of $I_{\rm in}$ with SHCM-PWM.

V. Conclusion

This paper proposed a new SHCM-PWM technique for grid-tied CHB active rectifiers. The proposed technique uses current reference instead of voltage reference to mitigate the current harmonics. It has been shown in the experiments that the actual utility grid has voltage harmonics, which can cause current

harmonic over the limit. Compared with SHE-PWM and SHM-PWM, the SHCM-PWM can mitigate the current harmonics due to grid voltage harmonics and mitigate higher orders of current harmonics with smaller inductance than the conventional SHE-PWM and SHM-PWM. This paper also explored the technique to analyze and design coupling inductance and switching frequency to meet current harmonic limits. Simulations and experiments were conducted to validate the proposed SHCM-PWM. The SHCM-PWM can greatly improve the performance of harmonic mitigation.

REFERENCES

[1] S. Khomfoi and L. M. Tolbert, "Multilevel power converters," in *Power Electronics Handbook*. Burlington, MA, USA: Academic, Aug. 2007, pp. 451–482.

[2] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4091–4106, Aug. 2015.

[3] S. Wang, R. Crosier, and Y. Chu, "Investigating the power architectures and circuit topologies for megawatt superfast electric vehicle charging stations with enhanced grid support functionality," in Proc. *IEEE Int. Elect. Veh. Conf.*, Apr. 2012, pp. 1–8.

[4] A. Moeini, H. Iman-Eini, and A. Marzoughi, "DC link voltage balancing approach for cascaded H-bridge active rectifier based on selective harmonic elimination-pulse width modulation," *IET Power Electron.*, vol. 8, no. 4, pp. 583–590, Apr. 2015.

[5] H. Zhao, T. Jin, S. Wang, and L. Sun, "A real-time selective harmonic elimination based on a transient-free, inner closed-loop control for cascaded multilevel inverters," *IEEE Trans. Power Electron.* vol. 31, no. 2, pp. 1000–1014, Feb. 2016.

[6] M. Sharifzade *et al.*, "Hybrid SHM-SHE pulse amplitude modulation for high power four-leg inverter," *IEEE Trans. Ind. Electron.* vol. 63, no. 11, pp. 7234–7242, Nov. 2016.

[7] C. Buccella, C. Cecati, M. G. Cimoroni, and K. Razi, "Analytical method for pattern generation in five-level cascaded H-bridge inverter using selective harmonic elimination," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 5811–5819, Nov. 2014.

[8] S. R. Pulikanti, G. Konstantinou, and V. G. Agelidis, "Hybrid seven-level cascaded active neutral-point-clamped-based multilevel converter under SHE-PWM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4794–4804, Nov. 2013.

[9] L. G. Franquelo, J. Napoles, R. C. P. Guisado, J. I. Leon, and M. A. Aguirre, "A flexible selective harmonic mitigation technique to meet grid codes in three-level PWM rectifiers" *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3022–3029, Dec. 2007.

[10] J. Napoles *et al.*, "Selective harmonic mitigation technique for cascaded H-bridge rectifiers with nonequal DC link voltages," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1963–1971, May 2013.

[11] A. Marzoughi, H. Imaneini, and A. Moeini, "An optimal selective harmonic mitigation technique for high power rectifiers," *Int. J. Elect. Power*, vol. 49, pp. 34–39, Jul. 2013.

[12] J. Napoles, J. I. Leon, R. Portillo, L. G. Franquelo, and M. A. Aguirre, "Selective harmonic mitigation technique for high-power converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2315–2323, Jul. 2010.

[13] A. J. Watson, P. W. Wheeler, and J. C. Clare "A complete harmonic elimination approach to DC link voltage balancing for a cascaded multilevel rectifier," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2946–2953, Dec. 2007.

[14] M. Dabbaghjamanesh, A. Moeini, M. Ashkaboosi, P. Khazaei, and K. Mirzapalangi, "High performance control of grid connected cascaded H-bridge active rectifier based on type II-fuzzy logic controller with low frequency modulation technique," *Int. J. Elect. Comput. Eng.*, vol. 6, no. 2, pp. 484–494, Apr. 2016.

[15] M. Najjar, A. Moeini, M. K. Bakhshizadeh, F. Blaabjerg, and S. Farhangi, "Optimal selective harmonic mitigation technique on variable DC link cascaded H-bridge converter to meet power quality standards," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 1107–1116, Sep. 2016.

[16] V. G. Agelidis, A. I. Balouktsis, and C. Cossar, "On attaining the multiple solutions of selective harmonic elimination PWM three-level waveforms through function minimization," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 996–1004, Mar. 2008.

[17] V. G. Agelidis, A. I. Balouktsis, and M. S. A. Dahidah, "A five-level symmetrically defined selective harmonic elimination PWM strategy: Analysis and experimental validation," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 19–26, Jan. 2008.

[18] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Std 519, 1992.

[19] A. Moeini and S. Wang, "Asymmetric selective harmonic elimination technique using partial derivative for cascaded modular active rectifiers tied to a power grid with voltage harmonics," in *Proc. Asia-Pacific Int. Symp. Electromagn. Compat.*, May 2016, pp. 982–987.

[20] M. Reyes-Sierra and C. A. C. Coello, "Multi-objective particle swarm optimizers: A survey of the state-of-the-art," *Int. J. Comput. Intell. Res.*, vol. 2, pp. 287–308, Mar. 2006.

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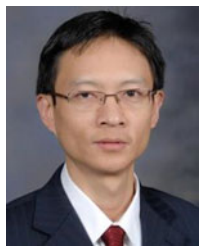

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